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Medium Voltage Solid-State Current Limiter

Test Results

Technical Report

Medium Voltage Solid State Current Limiter

Test Results

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Final Report, November 2006

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PRODUCT DESCRIPTION

Conventional circuit breakers have limits on the maximum current they are rated to interrupt. As more power is generated in order to provide energy for larger loads, circuit breakers can quickly become underrated for their fault current duty. Replacing these breakers is expensive, may require more space, and would cause significant disruption to grid operation because of extended outages. This report summarizes Solid-State Current Limiter (SSCL) developments during the past year. This three-phase, 15-kV, medium voltage device, rated at 1200-A, interrupts fault currents and limits the damage they could cause on downstream devices. In 2005, a three-phase prototype was designed and assembled, and initial tests were conducted to ensure that the power electronics operated properly. This report describes 2006 tests conducted to verify the device's current-limiting capabilities.

Results & Findings

This report will provide insight into the testing performed on the SSCL and its capabilities. SSCL advantages include:

- *New Capacity*—Fault current limiters could be applied to new capacity additions and/or positioned "surgically" at strategic locations, such as substation bus ties, to effectively mitigate fault current from multiple generation sources. This would provide a flexible tool that could be used to accommodate new capacity from generation, transmission, or distributed generation.
- *Grid Operations Alternatives*—The new functionality made possible by the flexibility of power electronics will also enable innovative alternatives in grid operation, with fault current limiters playing a key role.
- *Superconducting Cables*—A fault current limiter added in series with a superconducting cable can improve the cable's performance, permit design of smaller cable sizes, and eliminate loss of superconducting cable operation during cryogenic recovery time following an external fault.
- *Inrush Current*—The SSCL has a unique capability to limit inrush current, even for capacitive loads, by gradually phasing in the switching device. This may be of particular benefit in mitigating stress on generator shafts.

Challenges & Objective(s)

The key objective of this report is to provide a valuable tool for utilities to consider SSCL effectiveness. The SSCL's goal is to successfully interrupt any fault current during its rise before its peak value is reached. Challenges of SSCL development included ensuring its ability to limit

fault current and inrush current, while performing repeated operations with high reliability and without risk of component wear-out.

Applications, Values & Use

Current limiters have been used for low voltage systems, but were not economically viable for medium (5-kV to 38-KV) or transmission voltage (69-kV to 500-kV) systems. In the last decade, solid-state power devices have decreased in cost while improving performance, which has made it possible to produce a cost-effective SSCL. The SSCL operates in similar fashion to a circuit breaker, with the added ability to gradually stop the current flow. These advantages allow equipment, including circuit breakers, to remain in service while the fault current exceeds its rated value. The SSCL limits the current within a half cycle of the fault, while conventional circuit breakers only interrupt the current after about two and a half cycles. This quick response alleviates the short-circuit condition in both downstream and upstream devices by limiting fault currents coming from the sources of high short-circuit capacity. Furthermore, the SSCL can also limit the inrush current (soft start capability), even for capacitive loads, by gradually phasing in the switching device rather than making an abrupt transition from an open to a closed position.

EPRI Perspective

The SSCL is unique in that it is the first of its kind and takes an innovative approach to limiting fault current. The unique design of the SSCL enables it to limit the current based on its rate of rise as opposed to its amplitude. This feature provides an instantaneous (sub-cycle) current limit so that the system need never sustain the full impact of a fault current.

Approach

Initial tests on the SSCL were conducted at Powell Power Electronics Company in Houston, Texas, and recently, high power tests were conducted at KEMA Test Labs in Chalfont, Pennsylvania. Tests performed at Powell and at KEMA prove that the SSCL can protect downstream devices by effectively limiting the fault current. At Powell, capacitors were used to simulate a fault current to test the current-limiting abilities of a power electronic block (PEB) section, a complete phase, and two phases electrically tied together. These preliminary tests were performed successfully, demonstrating that SSCL controls and power electronics were functioning properly. The next step was to test the device's ability to limit an actual fault current created by a high power laboratory. Tests at KEMA confirmed that a 63-kA fault was successfully limited to approximately 20 kA. The final tests at KEMA then confirmed the SSCL's ability to limit 63-kA phase-to-phase, phase-to-neutral, and phase-to-ground faults. The SSCL device will soon be ready for a field demonstration.

Keywords

Solid-State Current Limiter
Fault Current Limiter
Current Limiter
Fault Currents

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1
INTRODUCTION

With more generators and larger transformers added to electric grids, fault currents reach extremely high damaging values that could risk the stability and safety the whole electrical system. These fault currents pose many problems to utilities including high dynamical and thermal stresses applied on its equipment such as overhead lines, cables, transformers, and switchgears. Fortunately, as fault currents have been exceeding in value, high power solid-state power devices continue to improve their capabilities and decrease in cost, which allows a Solid State Current Limiter (SSCL) to be a viable solution to electrical system problems created by high fault currents.

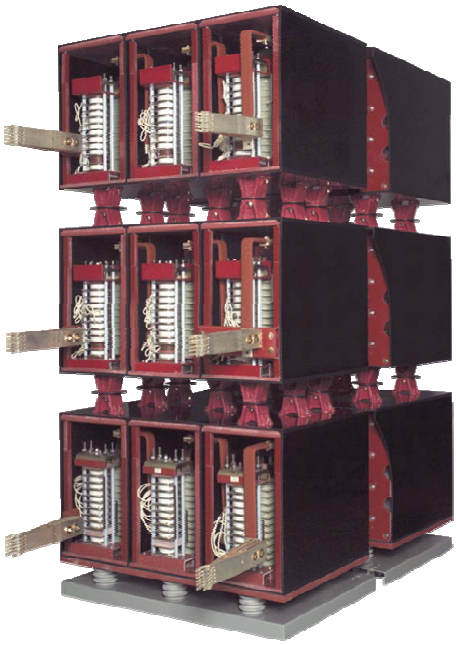


Figure 1-1
Solid State Current Limiter

The Solid State Current Limiter (SSCL) has been successfully tested during the last year (2006). These tests verified the unique ability of the SSCL to limit the current based on its rate of rise as opposed to its amplitude. Furthermore, since the SSCL has managed to limit a fault current up to 63kA in the laboratory environment without incident, the device will soon be ready for a field demonstration. A comprehensive report on the previous years work performed on the SSCL can be found in *Medium Voltage Solid-State Current Limiter, 2005 Progress Report. EPRI, Palo Alto, CA: 2005. 1010610.*

2
BACKGROUND

Solid-state current limiters consist of semiconductor devices such as GTOs (Gate Turn-off Thyristor), IGBTs (Insulated Bipolar Transistor), GCTs (Gate Commutated Thyristor), and thyristors. The thyristor was selected for the SSCL for various reasons including cost, availability, proven reliability, and application demands. The limiter's goal is to successfully interrupt any fault current during its rise before its peak value is reached. High fault currents are major contributors to the deterioration of transformer and electrical equipment life as well as power interruption and power quality. Current limiters have been used for low voltage systems, but were not economically viable for medium (5kV to 38KV) or transmission voltage (69kV to 500 kV) systems. In the last decade, solid-state power devices have decreased in cost while improving its performance which has made it possible to make a cost effective Solid State Current Limiter.

Power Circuit

The power circuit for the SSCL can be seen in Figure 2-1. The circuit consists of four main thyristors, TH1-TH4, and eight commutating thyristors, TH5-TH12.

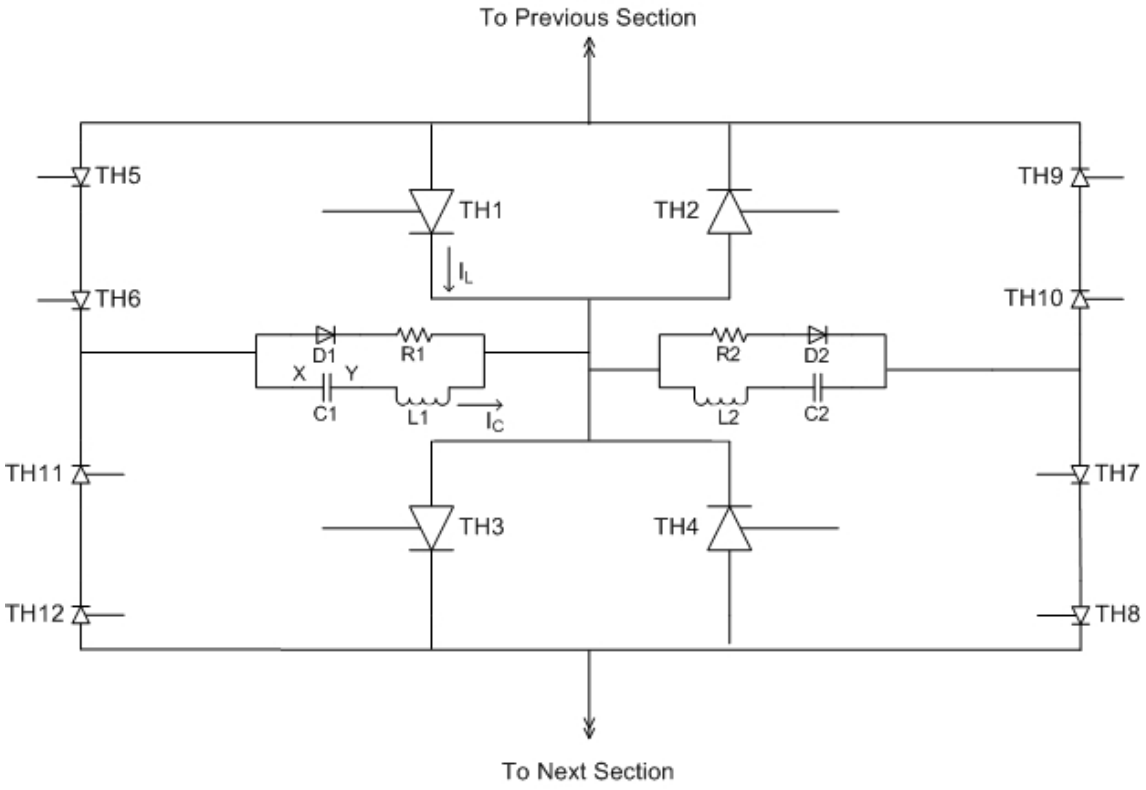


Figure 2-1
Power Circuit Schematic

The four main thyristors, or Silicon Controlled Rectifiers (SCRs), are controlled by four corresponding gate driver boards. Each gate driver is fiber optically connected to each other and uses firing pulses to turn each main SCR on. A current transformer monitors the bus' current and sends the status of each SCR back to the main phase controller. This controller sends signals to the gate driver boards to fire on the SCRs, depending on the current output.

In normal operation mode, the current flows through TH1 and TH2 or TH3 and TH4 depending on the direction of the current's flow. Initially as current flows, the capacitors charge, and the "Y' terminal holds a positive charge while the "X" terminal holds a negative one. When a fault current is detected, a "Turn On" pulse is sent to fire the commutating SCRs (TH5, TH6, TH7, TH8). The discharge current through TH 5 & 6, C1, and L1 build up, in order to exceed the load current, I_L, on the main SCRs. The current on the main SCRs, I_L, is eventually reduced to zero, and the excess of the commutating impulse current, I_C, flows through TH2. When TH2 turns on, the voltage across TH1 appears as an inverse voltage, and it turns off. After reaching its peak, the commutating current, I_C, starts to decay, and the capacitor charges with the opposite polarity ("X" positive with respect to "Y"). The commutating current then switches into the diode and resistor where it dissipates energy. Within a half-cycle the current crosses 0 and the commutating SCRs turn off.

The re-closing process begins by slowly phasing back the main SCRs to allow a short, limited pulse of current through the system. High firing angles are sent to the SCRs to allow a minimal amount of current to flow through the circuit. The limiter determines the line impedance from the current flow and if it is zero, or virtually zero, the fault current still exists and the main SCRs remain off to prevent the current from flowing. If there is impedance on the line, the limiter calculates the current and if the fault clears, the firing angle is slowly decreased to let more current through until eventually the four main SCRs are conducting in normal operation mode.

3
SUMMARY OF PREVIOUS WORK

Controls

The Solid State Current Limiter's ability to limit and ultimately interrupt the fault current is largely based on the system's control unit. The controls consist of different controllers, communication schemes, and detectors that collectively determine the limiter's course of action in the event of a fault current. A general diagram of the complete control scheme is illustrated in Figure 3-1.

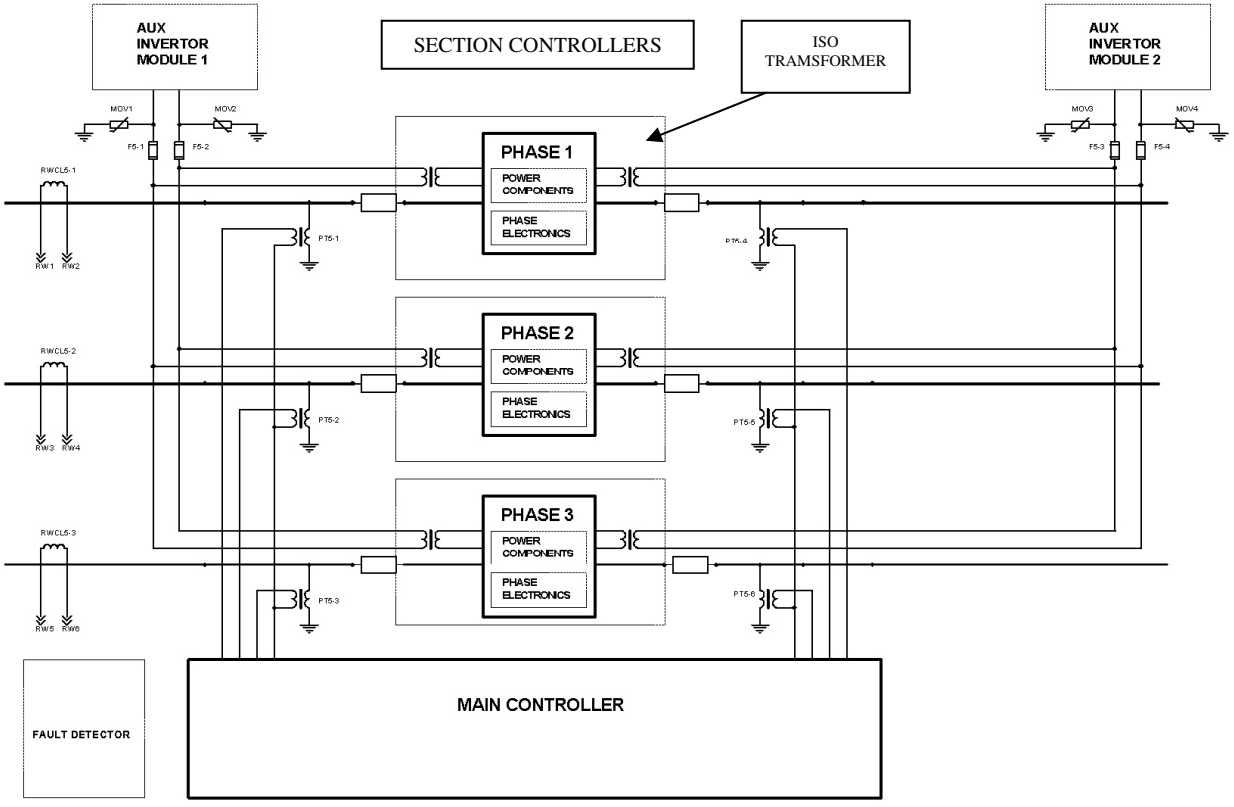


Figure 3-1
SSCL General Control Scheme

The auxiliary inverter modules provide power for the three section controllers on each phase of the device. The inverter supplies approximately 230 VDC at a high frequency (~30 kHz) in order to reduce the size of the high frequency isolation transformer connected to the section controller.

The Rogowski coils, shown connected on the left side of the phases in Figure 3-1, monitor the current through the SSCL. They produce the current's rate of rise (*di/dt*) as its output, and that information is fed into the fault detector. The fault detector filters the coil's output and then performs calculations inside the high speed controller to predict the future current value. The instantaneous current is determined by integrating the Rogowski coil's output. This value and a distinct amount of time, Δt, are inserted into the following equation, in order to determine what the current will be in the near future

$$i(t+\Delta t) = i(t) + \Delta t * (di/dt) \qquad \textbf{Equation 3-1}$$

Where,

$i(t)$ is the instantaneous current

If the current is expected to exceed set point levels, the "Turn-Off" signal will be fired by the fault detector's high speed controller and its Fiber Optic Drivers will send a signal to the gate drives through the fiber-optic cables.

Duplex fiber-optic cables are used to communicate between controllers and any device within the limiter. Fiber-optic cables are daisy chained through each phase and within all three sections of each phase as shown in Figure 3-2.

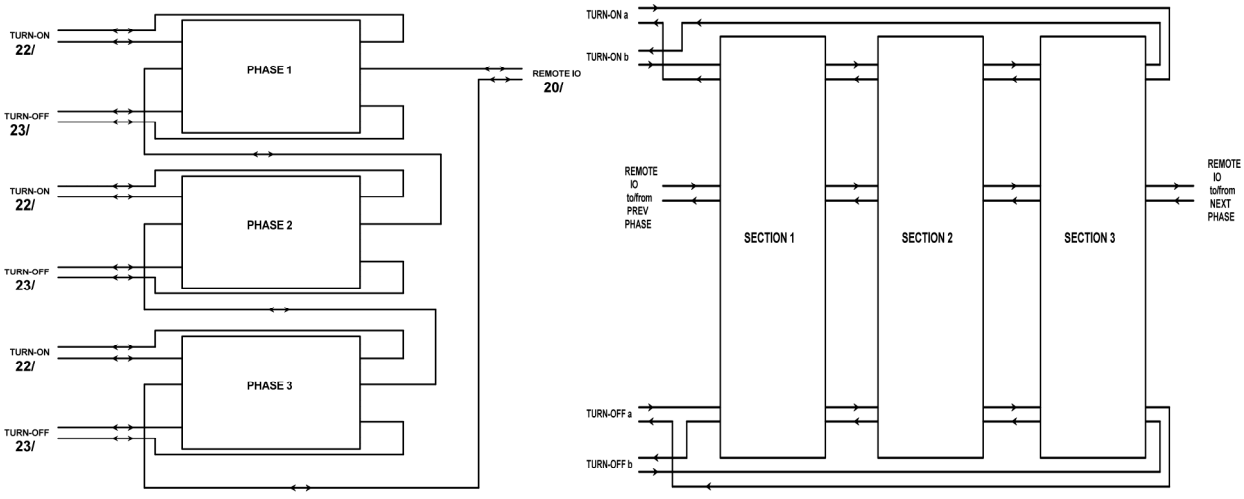


Figure 3-2
Fiber Optic Connections (Phase & Section View)

The duplex fiber optic cables allow information to travel in both directions through each phase and section. Duplex fiber optic cables were implemented to ensure that data will be able to be received or transmitted throughout the system even if one cable is bent, broken, or malfunctioning. Three distinct duplex fiber optic cables travel through the limiter labeled "Turn-On," "Turn-Off," and "Remote IO." The "Turn-On" signal is supplied from the main controller and sent to the section controller to turn on the main SCRs when the limiter is letting current through after it has stopped conducting, and when it is determining if the fault current still exists during the re-closing process. In the event of a fault, the "Turn-Off" signal is generated from the fault detector and sent to the section controller to turn on the commutating SCRs. The "Remote IO" cables control and monitor the fans, capacitor voltage, and temperature of all nine sections in the SSCL.

The section controller monitors and executes all of the commands within the Power Electronic Block (PEB) or section. It sends signals to the main and commutating gate drives in order to turn the main or commutating SCRs on and regulate the fan speed. It also provides power to the capacitor pre-charge module, the main and commutating SCRs, and the sections fans. Furthermore, the section controller monitors the voltage of the capacitor pre-charge module and the nine conducting cables through the commutating conductors. The fan drive is monitored by the section controller with respect to the current on the section bus. The current transformer on the section bus supplies energy for the fan drive thereby adjusting the speed of the fans as required.

Testing

Several tests conducted over the years provided data on the performance and effectiveness of the Solid State Current Limiter, and they also help determine the stability of the limiter's structure and design, and were also conducted in order to verify the current limiting capabilities of the limiter.

Basic Impulse Level Withstand Test (BIL)—July 25, 2005

The preliminary Basic Impulse Level withstand test (BIL) for the Solid State Current Limiter (SSCL) was performed to determine the dielectric strength of the limiter given a large voltage surge. Due to the unique design of the SSCL, there were no guidelines or standards to govern the design testing procedures or expected outcomes on this prototype. Therefore, high voltage AC breaker standards were used to create the following test plan. Some of the standards utilized for this test plan were ANSI C37.09-1999 and ANSI C37.06-2000. This test provided data that should verified that the component spacing and positioning of the hardware in one complete phase is adequate and will withstand the voltages described in ANSI C37.09-1999.

Phase A was energized across the power leads; while Phase B and the Base Cart (Ground Plane) are grounded. The criterion for pass/fail is the non-occurrence/occurrence of a flashover to ground. The testing position of the unit's SCR's is in the naturally "OFF" position because all control circuits and gate controls for the device were removed. All the gate and control lead

were tied together and isolated to prevent damage to any of the SCRs during the test. All of the primary circuit components were electrically tied together so that they all would be energized and we could observe the effects of the test on all major components. Three positive and three negative impulses of 95 kV are applied on the bottom phase of the limiter, and the voltage discharge is observed over time.

According to IEEE Std. 4, a 15kV device should be able to withstand a 95kV BIL test. Due to the atmosphere and temperature of the testing facility, the SSCL was struck with 98kV so that a true 95kV voltage was attained. After the initial voltage strike, the unit must uniformly decay 50% of the peak voltage within 50µs (+/-20%). Both positive and negative strikes illustrated on Figure 3-3, and they discharged to ~49kV within 49.64µs. Since the graphs show a uniform decay and the time to discharge was within 50µs, the SSCL passed the test.

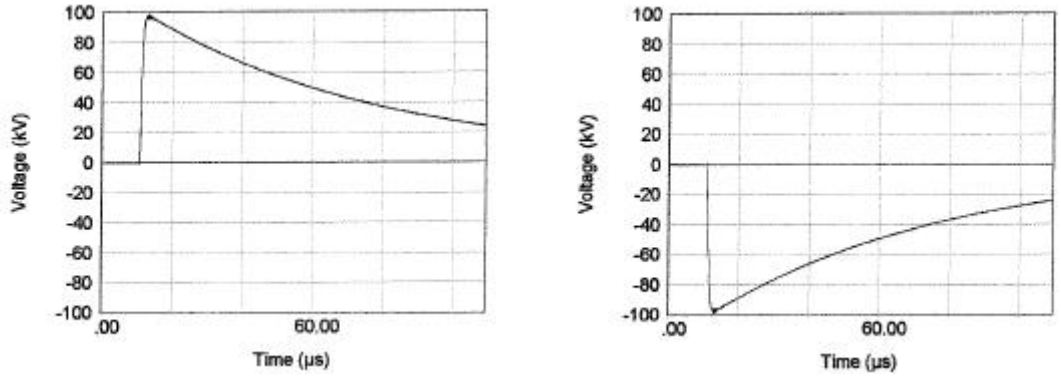


Figure 3-3
Impulse Withstand Test Results

Partial Discharge Test—July 25, 2005

The Partial Discharge test was developed also with consideration of ANSI C37.09-1999. Using the same test setup that was used for the BIL test, we applied a voltage of 36 kV for one minute. Coulomb measurements are taken during the test measuring any partial discharge that may be present. The results of the dielectric tests described above will provide vital information on the overall dielectric capability of the SSCL.

As seen on the graphs in Figure 3-4, there was no partial discharge during the test. Due to noise associated with the testing equipment, three spikes appear on the waveform, but it does not indicate any partial discharge problem. The PD instruments measured 7pC of background noise and no detectable partial discharge at approximately 11kV. According to ANSI C37.09-1999, for 15kV devices the extinction voltage must be greater than 10.5kV, and we recorded an inception and extinction voltage above 32kV. Above 32kV the average partial discharge measured above 299pC. As seen in the bottom graph on Figure 3-4, the voltage was raised to 32kV and held for one minute.

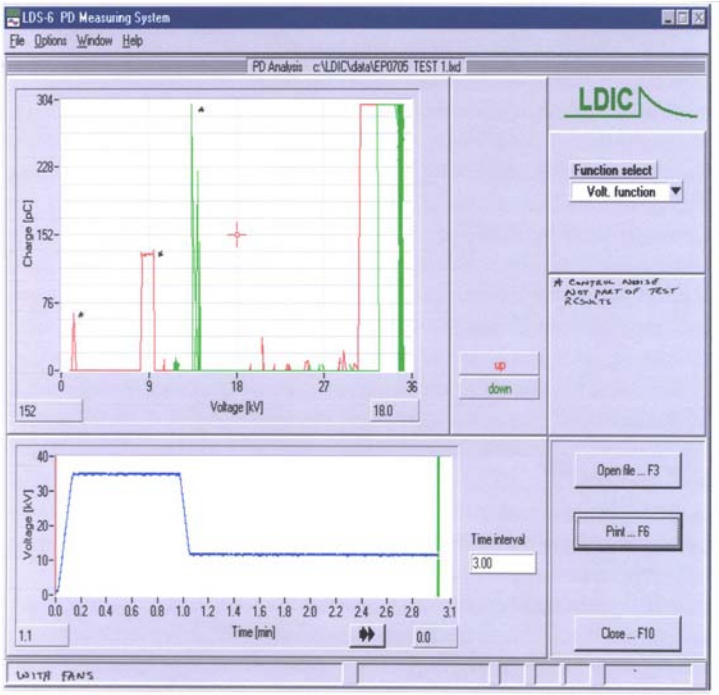


Figure 3-4
Partial Discharge Test Results (with Fan Compartment)

The voltage was then decreased to approximately 10kV and held for two minutes. A successful test is denoted by partial discharge characteristics at the extinction voltage (32kV), but the characteristics should disappear when the voltage is beneath the extinction voltage. Figure 3-4's top graph shows the observed charge as the voltage is increased and decreased. Partial discharge effects occur at approximately 32kV, as expected, and returns to normal levels below 32kV.

Continuous Current Bench Test—September 12, 2005

Fan Air Pressure

A power transformer provides a step down voltage, 480 to 16.5 volts, across one phase of the SSCL (only one phase tested). The 16.5 volts across the middle phase of the SSCL creates a 1200A current conducted through all four main SCRs. A diagram and picture of the set up can be seen in Figure 3-5.

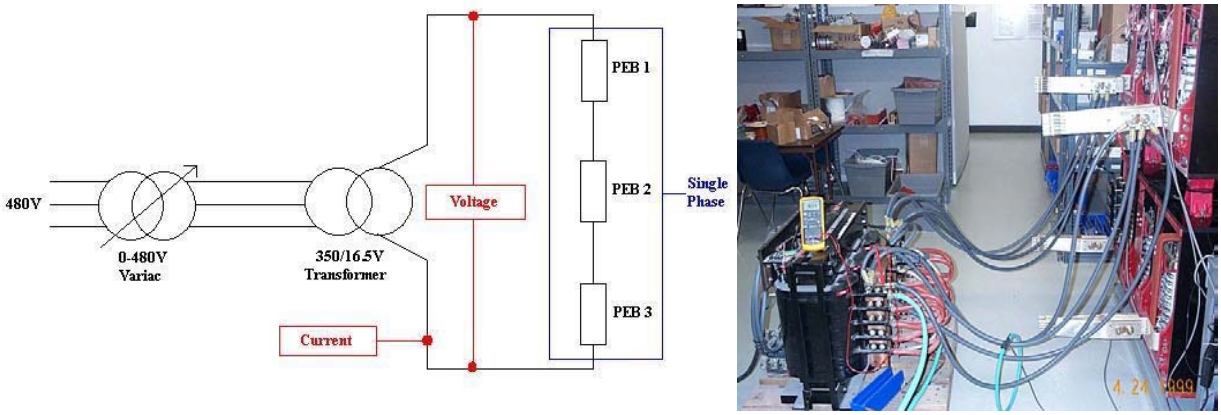


Figure 3-5
Current & Voltage Measurement Scheme

While the SCRs were conducting 1200A, tests were performed measuring the air pressure inside an SSCL compartment with respect to the air in the test facility. Two test trials were completed, one with two fans on per phase and the other with all three fans on per phase. A manometer measured the difference in the air pressure inside the middle phase of the current limiter and outside the limiter, in the testing room. The tests recorded 1.3 inches of water displacement for the two-fan test and 1.5 inches for the three-fan test. These results were used to calculate the maximum temperature allowable for the SCRs to operate while conducting continuous current.

Continuous Current Test—October 13, 2005

Unfortunately, due to the innovativeness of the Solid State Current Limiter (SSCL), specific standards and limits for a continuous current test currently do not exist. Therefore, in order to have some guidelines for the SSCL's continuous current test, the IEEE standard for Metal-Clad Switchgear was used as a model for determining temperature limits for various components of the current limiter because it most closely matched the purpose and design of the SSCL. Specifically, the test procedure and requirements adhere with reference to IEEE Std. C37.20.2-1999 and an established a maximum temperature limit of 85°C for any SCR.

Thermocouples measure the temperature of various components of the SSCL. They are placed in intimate contact with the surface it is measuring with self adhesive material connecting it to the surface. The continuous current test of the Solid State Current Limiter measures the temperature of the heat sinks and SCR cases.

As seen in Figure 3-6, two SCRs from each Power Electronic Block (PEB) have thermocouples strategically placed to read its temperature. The leftmost PEB has thermocouples on the top two SCRs, the middle PEB has them on the second and last SCR, and the rightmost PEB's thermocouples reads the temperature of the bottom two SCRs. Three other thermocouples measure the ambient temperature outside the SSCL enclosure and in the other two phases of the

limiter. The last thermocouple was placed on the copper fork that connected to the source transformer.

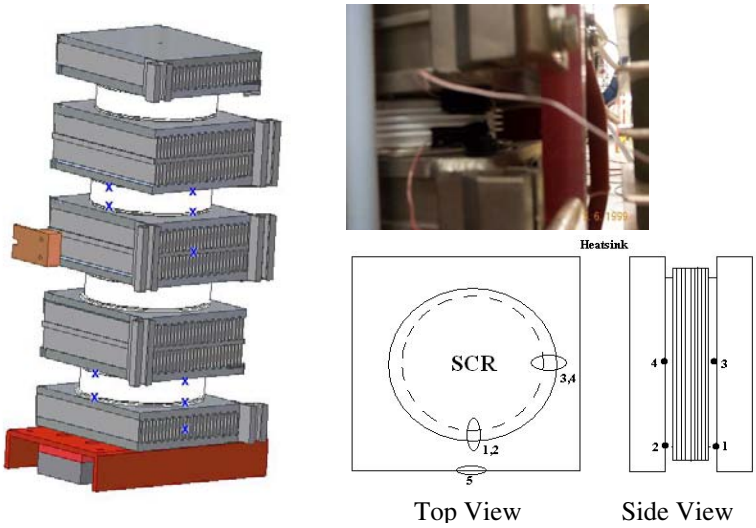


Figure 3-6
Thermocouple Placement

The tests are executed with eight fans operating. The ninth fan, on the top phase, is currently not operating and has been temporarily replaced with a nonmagnetic barrier so that air will not cause a short circuit around the non-operating fan.

A continuous current of up to 1200A is applied to the system until the temperature rise of any monitored point does not change by more than 1 °C over a one hour period, with readings being taken at least every 30 minutes. The equipment is considered to have passed the test if the temperature limits defined by IEEE Std. C37.20.2-1999 and the SCR case has not exceeded 85°C. For this first preliminary series of tests, only the SCR case temperature limit was considered since it was the worst case scenario.

Results

As the middle phase conducts a continuous current of 1200A, the SCRs' heat sinks peak at temperatures over 85°C. After carefully examining the results of the test and the SSCL, itself, it was determined that the air inside the enclosure was just circulating within the limiter, as a result the temperature kept increasing. The air flow was not effectively directed out of the SSCL, so nonmagnetic barriers were placed between each phase to block the air from traveling back to the capacitor bank inlet.

Different variations were created in order to try and force the hot air out of the SSCL's enclosure. The most effective method was obtained with the non-metallic barriers in place and with the top vent removed. This arrangement provided the maximum temperature relief and

peaked at about 67°C. The barriers were removed, however, due to dielectric concerns. The resulting setup with the top vent and non-metallic barriers removed created an environment of about 75°C. It appeared that as the discharge airflow area increased in the top of the enclosure, the air flow was more effective and the temperature of the SCRs decreased significantly. Although measured SCR case temperatures were below the established limit of 85°C, a final conclusion could not be determined until the complete three-phase continuous current test was completed.

4
SUMMARY OF WORK IN 2006

Factory Testing

Capacitor Discharge Current Limiting Test

In order to test the power electronic assemblies under realistic conditions, a source with substantial short circuit power is needed. To simulate an 80 kA fault at 13.8 kV, 1900MVA will be required. Assuming a sub-synchronous generator impedance of 17%, a generator with rated power of 320 MVA could provide that fault current condition. Even if a single section at 1/3 of the voltage level is tested, the required rated power of the generator is above 100 MVA. This type of test is extremely difficult to perform in facilities not normally equipped with this type of equipment; therefore, plans have been arranged for the test to be conducted at a High Voltage laboratory (KEMA). However, it is necessary to provide production and design testing to first verify operation of the current limiter before going to KEMA because with power up to 100 MVA any minor problem could seriously damage the unit.

To provide some preliminary current limiting tests results, a fault current will be simulated using the SSCL's capacitor banks. Four complete capacitor phases are built in order to simulate the fault current. The combined capacitors of three phases are used to form a capacitor bank to test the 4th phase. The capacitor banks from individual sections are connected in parallel and an inductor is used to simulate fault impedance. An air inductor made from jumper cable is created to make the required 100 μH inductance for single section testing and 300 μH for complete phase testing. These inductors require less than 10 turns.

Single Section Testing—November 2005

This important test will have to occur for every produced section. In this test both maximum voltage and current levels are simulated to verify operation of power and control components.

The required voltage level is

$$V_{\max} = \frac{1}{3}\frac{V_{line}}{\sqrt{3}}\sqrt{2} = 4.13\ kVpk \quad for\ V_{line} = 15.2\,kVAC \qquad \textbf{Equation 4-1}$$

Three sections are connected in series, so that the voltage per section is 1/3 of total, or 4200 V. To simulate the 80 kA fault interruption, the same appropriate impedance should be in the test circuit as in a real fault condition; therefore at 80 kA symmetrical fault the *di/dt* is

$$\frac{di}{dt}_{\max} = I_{fault} \cdot \sqrt{2} \cdot 2\pi f = 42.6 \frac{A}{u\sec} \qquad \textbf{Equation 4-2}$$

To achieve this *di/dt* at 4200 V an inductor of 100 uHy will be required.

With this inductor the peak uninterrupted current is about

$$I_{pk} = V_{\max} \cdot \sqrt{\frac{C}{L}} \qquad \textbf{Equation 4-3}$$

In this case V_{max} is 4200 V, combined capacitance of three phases is 12000 μF and the inductance is 100 μH.

$$I_{pk} = 46.7kA \qquad \textbf{Equation 4-4}$$

This value is high enough to allow complete testing of the section, including noise immunity and actual current interruption, and it is within current withstand capability of the SCRs. So even in the case of a malfunction, the SCRs are more likely to survive the fault. The current interruption in the main SCR occurs within a few hundred microseconds, and the current limiting action can be verified. Since 1/3 voltage level is used to test, the standard voltage probes and isolators are used to get complete pictures for voltages and currents in the section. The test setup is shown on Figure 4-1.

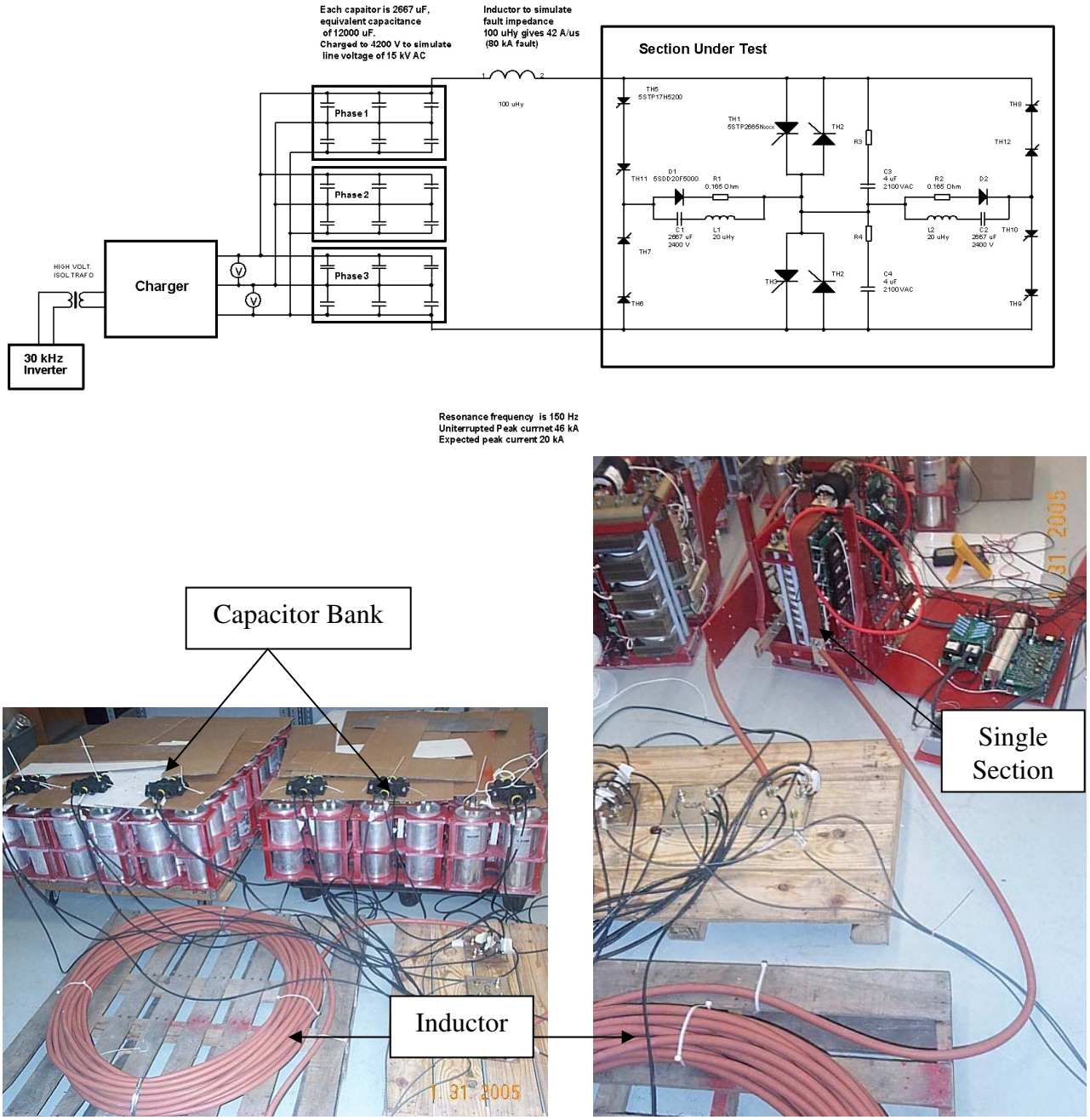


Figure 4-1
Capacitor Discharge Single Section Test Setup

The tests are conducted by first charging the capacitors to approximately 1000V. Next, a fault current is simulated by turning on the main SCRs which discharges the capacitors. This simulated fault current is represented by the "Main SCR Current" curve in Figure 4-2. The fault current flows through the main SCRs and the inductor. As the main SCRs conduct the fault current, the commutating SCRs interrupt the fault current by producing current in the opposite direction. The fault current reduces to zero and the excess energy dissipates into the inductor load.

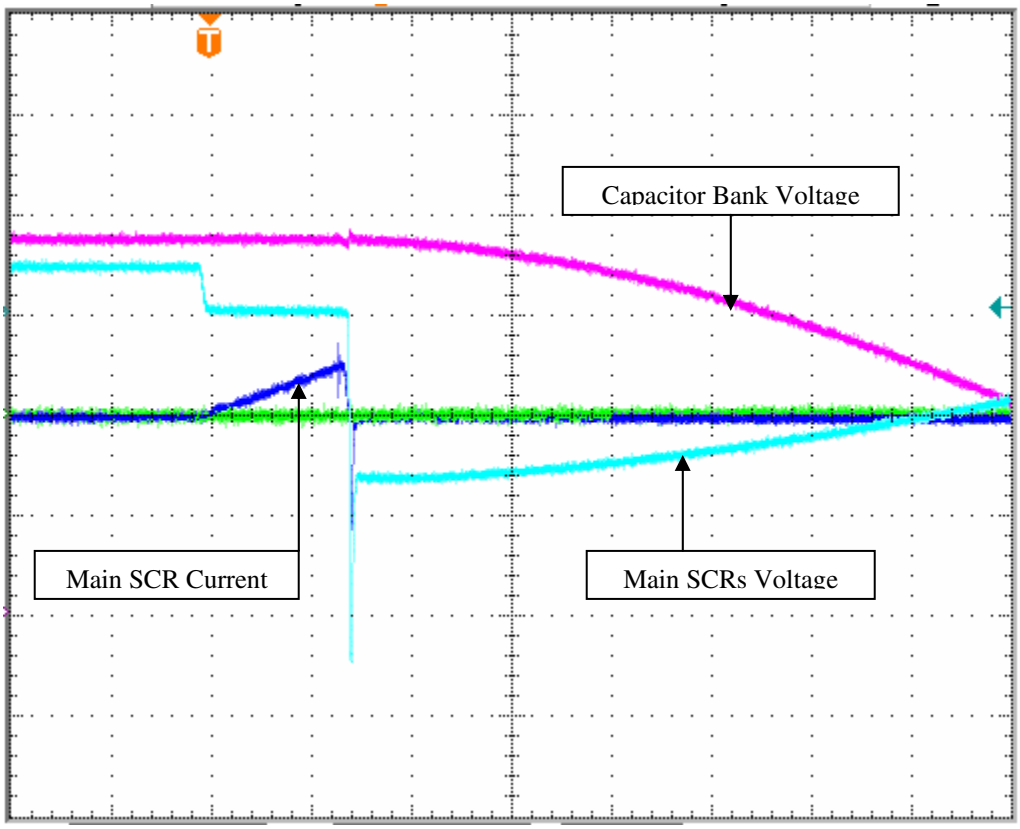


Figure 4-2
Capacitor Discharge Test—Waveform Output

Initial testing has shown that an undesired voltage spike occurs when the main SCRs turn off. These voltage spikes were comprised of a high voltage rate of rise (*dv*/*dt*) which consequently caused pre-mature firing of the SCRs during commutation. This issue required the main SCR snubber circuits to be redesigned to limit the voltage spikes and the corresponding high *dv*/*dt* values to a safe level.

After the snubber circuits were replaced, the tests first continued with a test of only a half section at full voltage and current. Only the half section was tested as a precaution to avoid damage to other part semiconductor devices. In order to simulate an 80kA symmetrical fault, the current's rate of rise should be about 43A/μs. The total series inductance was adjusted to simulate the required *di*/*dt*. The half-section successfully interrupted the 4800A, 2000V current, and then the complete power section was restored and tested at 4800A and 4000V. The section for both voltage/current polarities was verified. The test results can be seen in Figure 4-3.

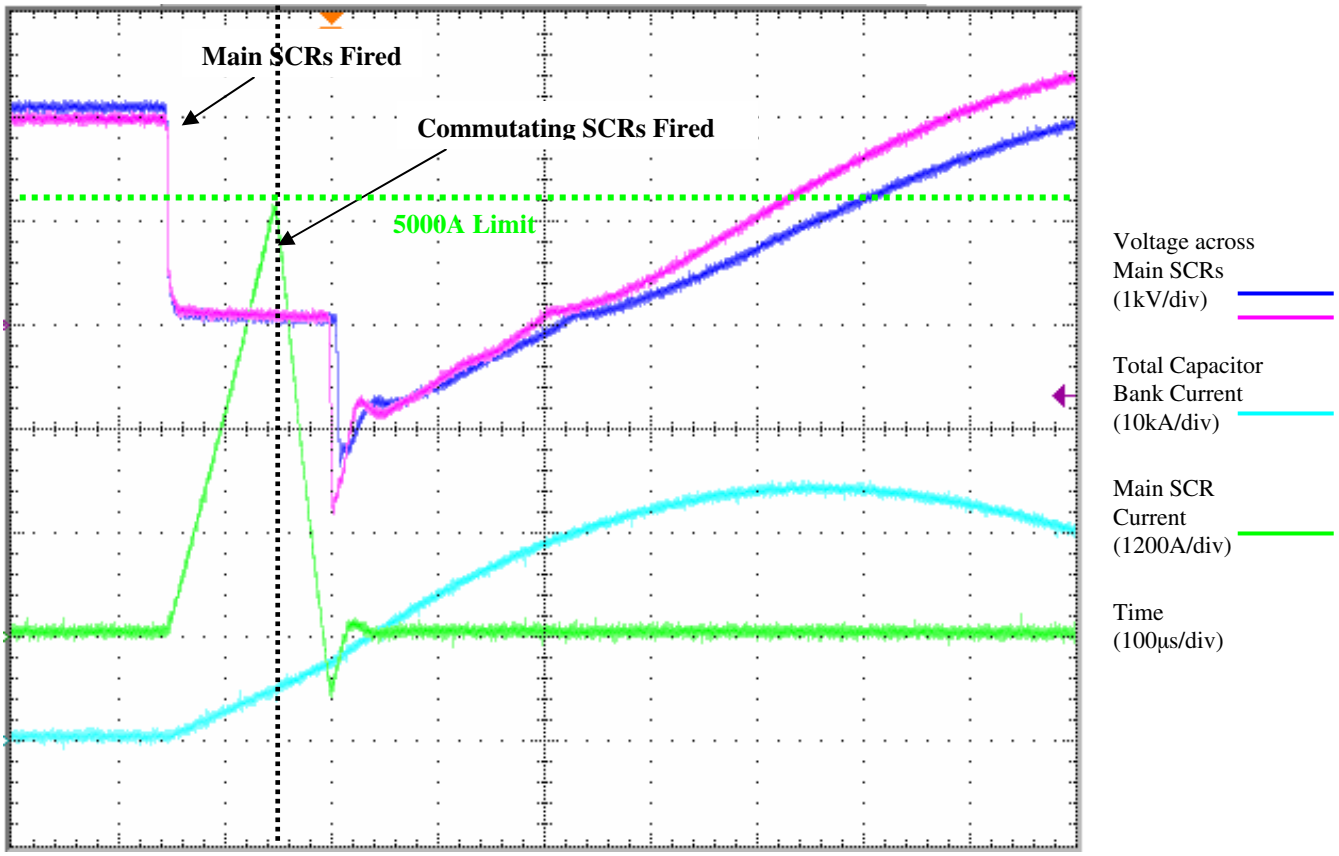


Figure 4-3
Single Power Electronic Block Current Interruption

It can be seen in this figure that when the main SCRs are fired, the current across the main SCRs immediately rises with a sharp rate of rise (di/dt). The high di/dt triggers the fault current detector in the controls as described in chapter 2. The fault current detector sends a signal to the commutating SCRs to turn on and as a result, the current through the main SCRs dropped to zero within ~50µs. The test established the Power Electronic Block's (PEB) ability to successfully interrupt the current based on the current's rate of rise. The next step in testing is to combine three PEBs in series in order to form a complete phase and test the current interruption capabilities of the SSCL on a phase.

Single Phase Testing—March 2006

Single phase testing initially encountered a few problems that inhibited the limiter from operating properly. As three PEBs were connected together, the section controllers were losing communication with the main controller. After thoroughly investigating the problem, it was determined that there was a software problem that caused a program to overwrite certain data with measured values. As a result, the behavior was unpredictable and the crash occurred more often while the unit was running in the presence of high noise level. This software glitch was corrected and the communication was consequently functioning appropriately.

Other problems occurred in the electronics attached to each PEB including the destruction of a gate drive pc board. The driver board was picking up noise during power up, and as a result both IGBTs in a leg were turned on at the same time, creating a short circuit across the capacitor filter. As a result, the IGBTs are destroyed with the high current which in turn destroys the driver circuit and the pc board. Consequently, the controller board is exposed to high voltage and many other components are destroyed as well. The damage incurred on the circuit can be seen in Figure 4-4.

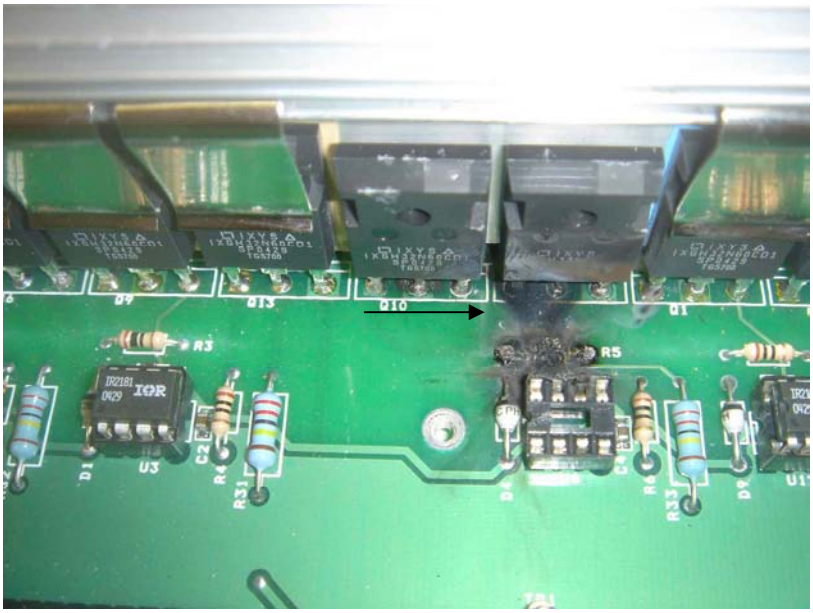


Figure 4-4
PC Board Damage

Additional circuitry had to be developed to filter the noise on the driver board. A test setup was also created to power the section controller. The controller was powered up and down over 1000 times to ensure that the problem was resolved.

After the communication was verified between the controllers, the three modules (PEBs) were connected in series with an applied capacitor bank voltage of 12kV with a di/dt of 45A/μs. The single phase setup for this circuit is diagrammed on Figure 4-5. As stated earlier, this rate of rise will simulate an 80kA fault at line voltage 14.7kVAC and 90° phase shift. Five pulses at full voltage and current were initiated in each direction, and the typical results can be seen in Figure 4-6.

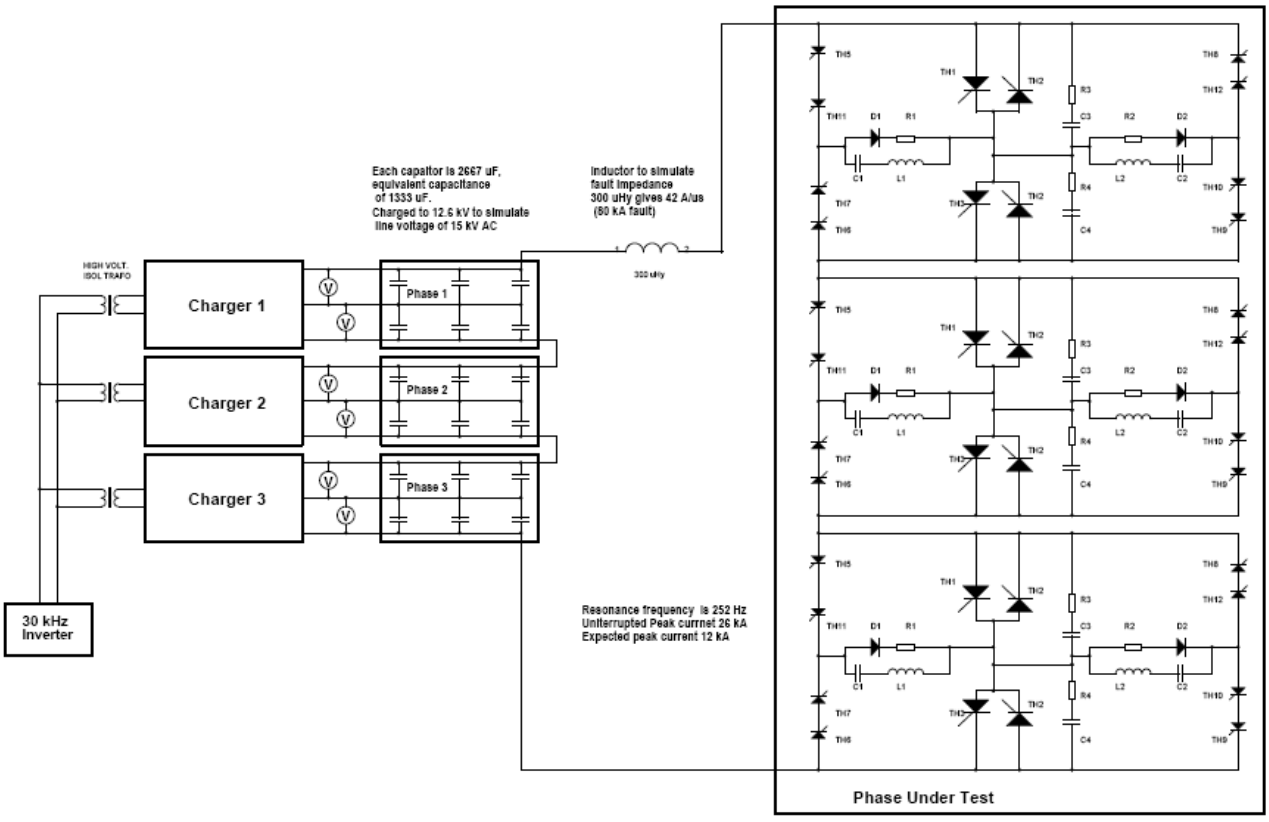


Figure 4-5
Single Phase Test Setup

The current through one section's main SCRs is limited approximately 80μs after the fault was induced. The current and voltage traces resemble the curves obtained from the single section graph in that the fault current rises as the main SCRs are turned on. After the commutating SCRS are fired, the fault current declines, and the main SCR voltage drops again shortly after. The phase unit performed reliably during the 23 pulses. No communication glitches were recorded between the section and main controllers.

The single phase testing did not, however, go without incident. Several capacitors failed during the initial section test pulses. In one case the capacitor opened while carrying high current causing a small explosion inside the capacitor. After verifying that the capacitor voltage and current in the circuit were well within the capacitor specifications, we contacted the capacitor manufacturer for a further investigation on the problem. It was determined that the inductor above the capacitor section was producing a magnetic force that was pushing down or up on the capacitor poles. This force caused the break point inside the capacitor to fail which led to capacitor failure. The inductor wiring was re-routed to minimize these vertical forces with no subsequent capacitor problems. A future design improvement will be to use a capacitor without a breakpoint element.

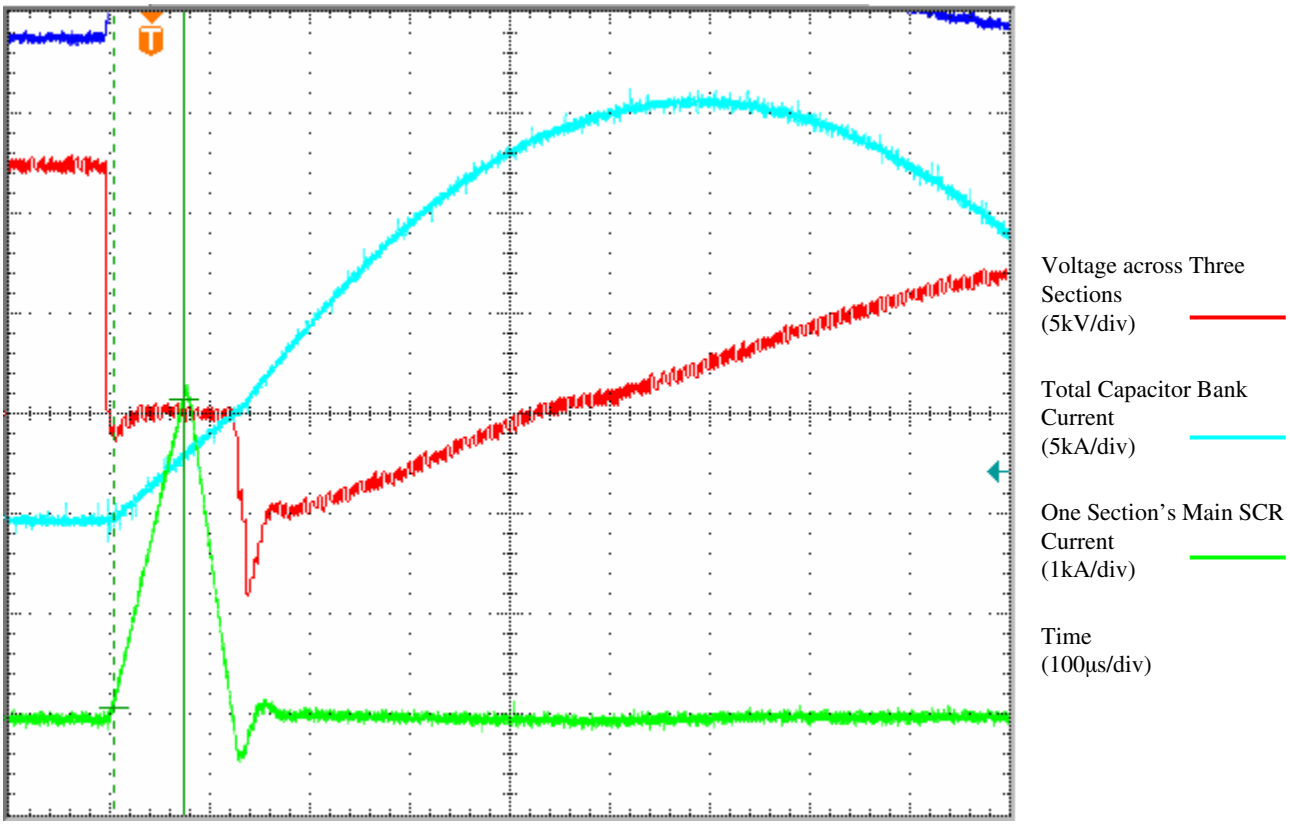


Figure 4-6
Single Phase Current Interruption

Prior to the capacitor failures, the magnetic field generated by the inductor was causing the connectors between the PEB and capacitor sections to disengage. After further investigation, it was determined that the pulse that occurred during the capacitor discharge caused the wire retainer inside the capacitor to fracture. The current design amended the problem by making use of copper clips and knife blades in place of the pins. The clips allowed for a rigid mounting to each section.

Another issue included the finding of a wire lug size that was not suitable for the multiple strand wire used as an inductor in the capacitor cart. During the current interruption process, the wires snapped out of its respective lugs due to the current absorbed by the inductor. Different methods such as soldering the lug onto the wire, crimping the lug with various tools, and using wire tie downs did not keep the wire connected. A larger lug size was finally used for the multiple strand wire. When purchasing the new lugs, the tool and die stamps were also purchased to ensure the wire and lug connect is secure. Future designs will revisit this issue to make these terminals even more robust. The damaged inductor lugs can be seen in Figure 4-7.

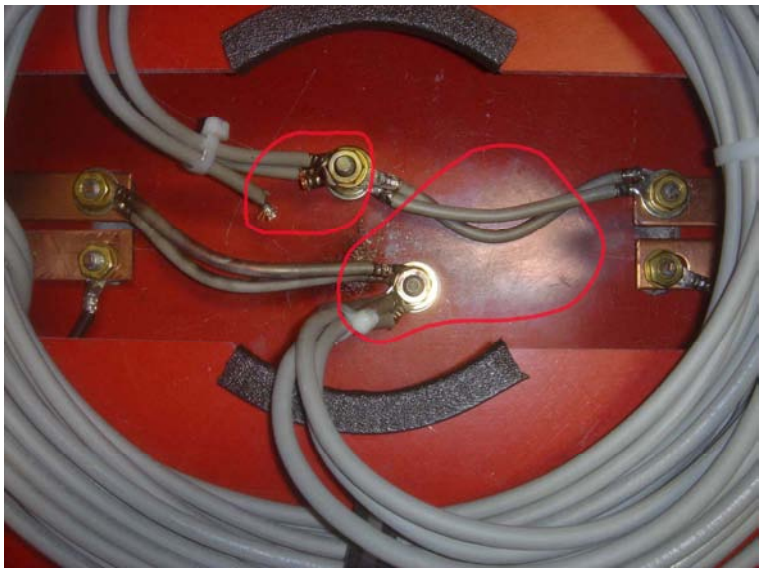
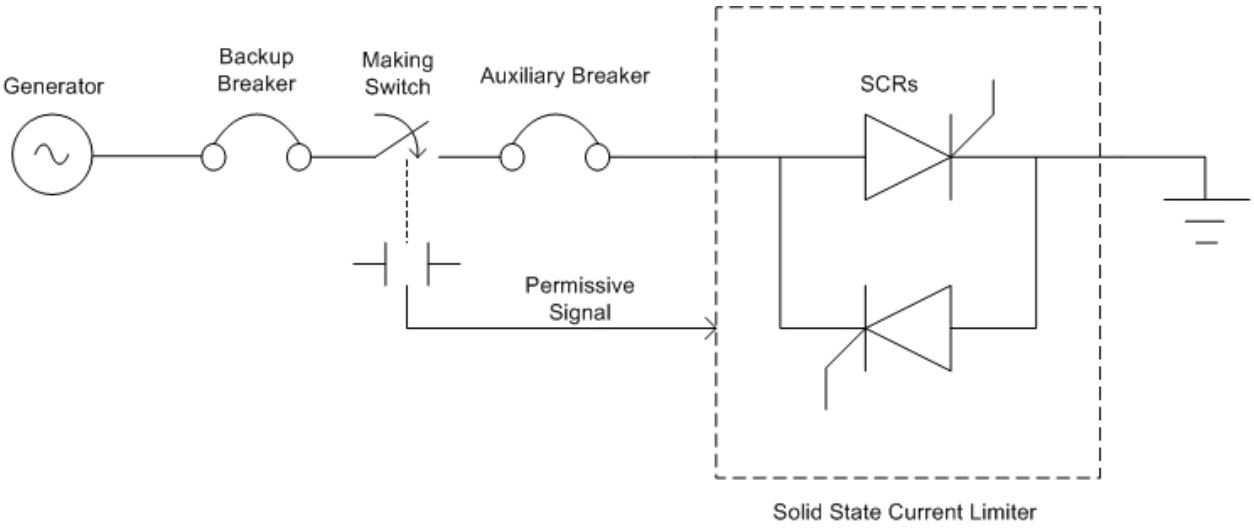


Figure 4-7
Damaged Inductor Lugs

KEMA High Power Testing—September 2006

Prior to the high power testing conducted at KEMA, four complete phases (12 sections) were thoroughly tested in the factory using the test procedures described earlier. The KEMA tests were designed to prove that the Solid State Current Limiter could interrupt a phase-phase, phase-ground, and a three-phase fault current of up to 63kA. Four complete phases were assembled so that one auxiliary phase would be available in case a problem arose with any of the other phases or PEBs for that matter.

The test setup at KEMA, illustrated on Figure 4-8, uses a 2,250 megawatt generator to create a fault current of about 63kA. The backup and auxiliary breakers are used as protection devices on the fault current in case the SSCL fails to limit the current. These two breakers are closed prior to the current pulse, while the "making switch" is open. Initially, the SCRs inside the limiter are turned off until the "making switch" sends a permissive signal to the current limiter which enables the SCRs to start conducting, even though there is no current flow from the circuit. While the SCRs are conducting, the making switch is closed producing the fault current across the SSCL. For safety concerns, the auxiliary breaker opens shortly after the fault, but the SSCL limits the current before the auxiliary breaker opens.



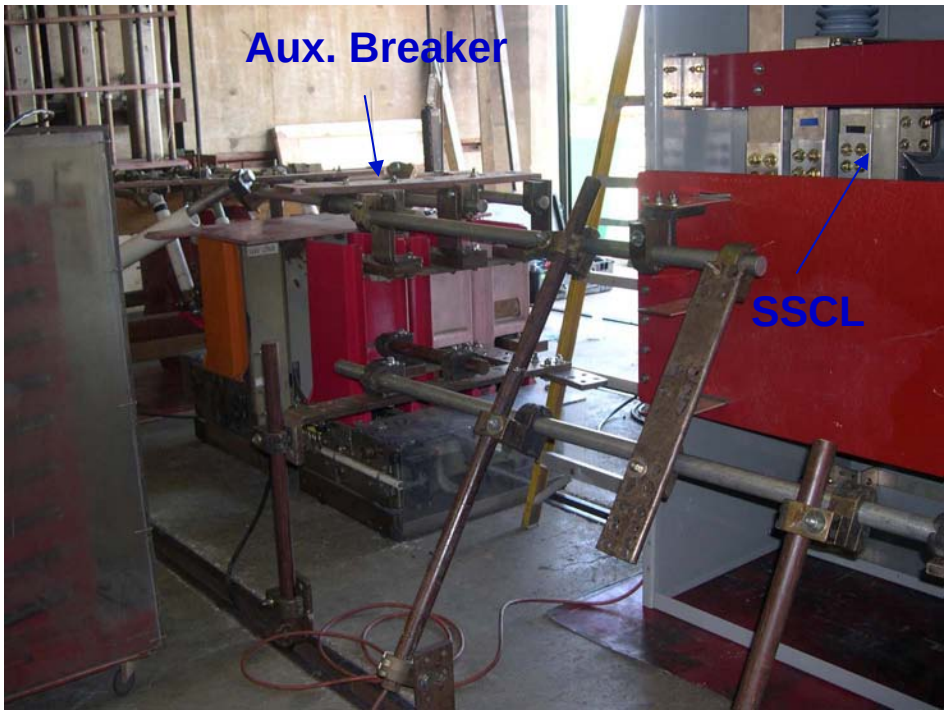
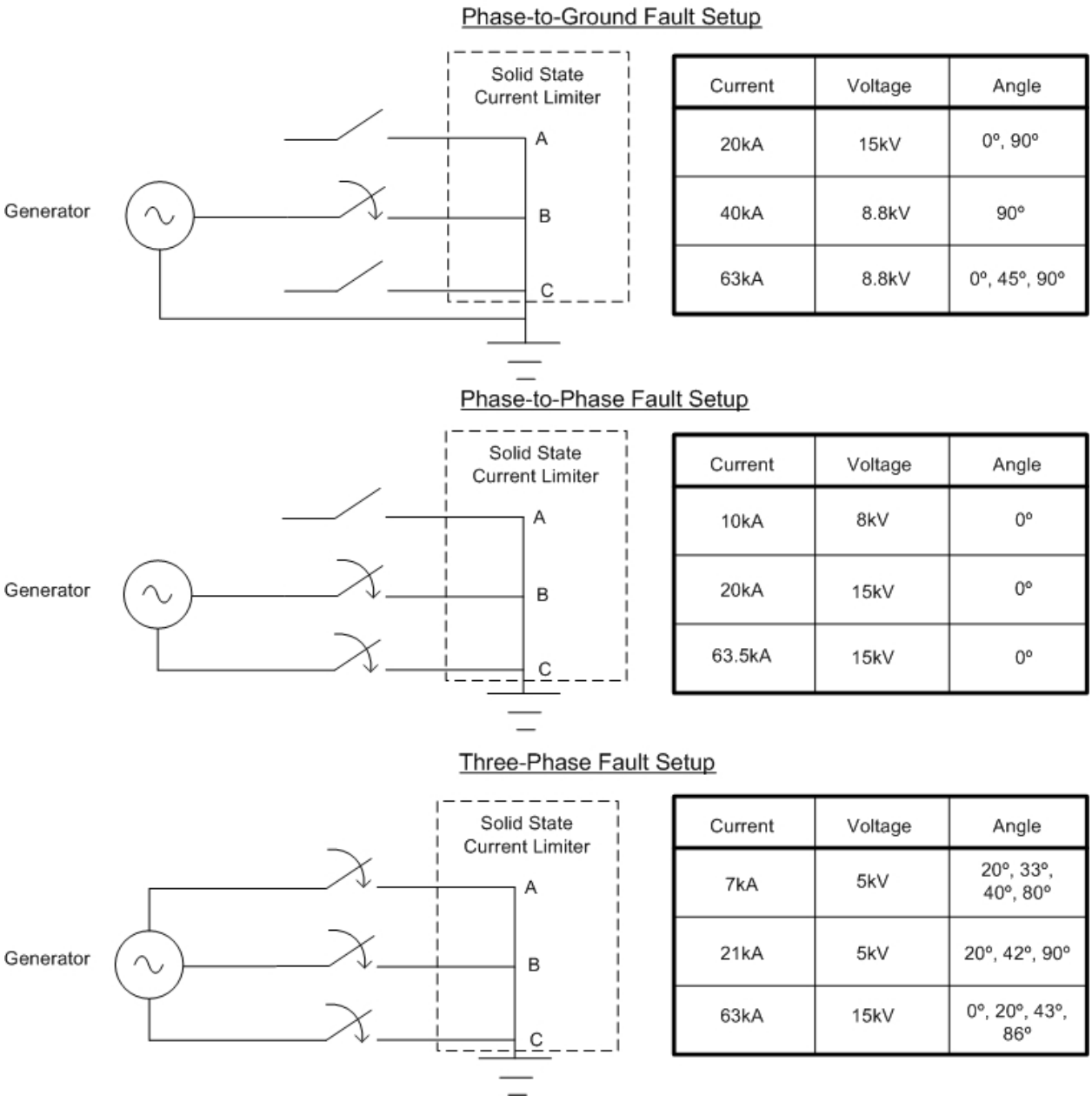


Figure 4-8
KEMA Test Setup

The SSCL is connected as per the diagram shown in Figure 4-9, in order to simulate a phase-ground, phase-phase, and a three-phase fault. Each fault setup is tested with faults that range from 7kA-63kA and 5kV-15kV at various angles. A list of test currents, voltages, and firing angles are listed on Figure 4-9.



Current	Voltage	Angle
20kA	15kV	0°, 90°
40kA	8.8kV	90°
63kA	8.8kV	0°, 45°, 90°

Current	Voltage	Angle
10kA	8kV	0°
20kA	15kV	0°
63.5kA	15kV	0°

Current	Voltage	Angle
7kA	5kV	20°, 33°, 40°, 80°
21kA	5kV	20°, 42°, 90°
63kA	15kV	0°, 20°, 43°, 86°

Figure 4-9
Test Fault Current Parameters

The Solid State Current Limiter's typical reaction to a fault current is diagrammed in Figure 4-10. In order to fit the phase "C" current, phase "A" current, and the main SCR voltage on the same oscilloscope screen, the phase "C" current waveform was inverted.

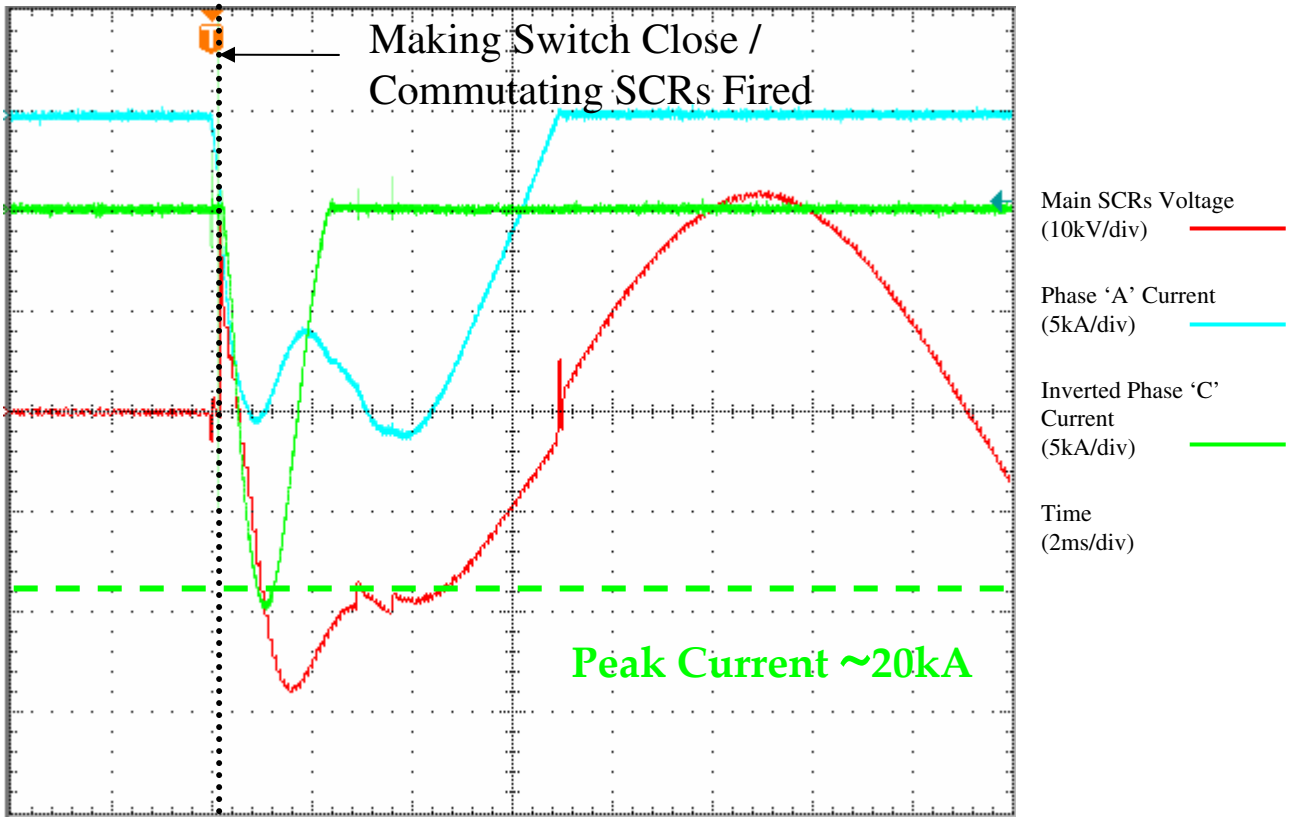


Figure 4-10
SSCL Three-Phase 63kA at 0° Fault Interruption

Figure 4-10 details the SSCL's ability to limit a three-phase, 63kA fault at zero degrees. The main SCRs are turned on before the making switch closes because the permissive signal allows the SCRs to start conducting. Once the making switch closes the fault current through phase 'C' rises steeply, and the corresponding slope of this current increase, or the current's rate-of-rise (*di*/*dt*), triggers the fault detector controller to fire the commutating SCRs. The energy stored in the SSCL's capacitors is released and its current flows against the main SCR's fault current. This process is illustrated in Figure 4-11.

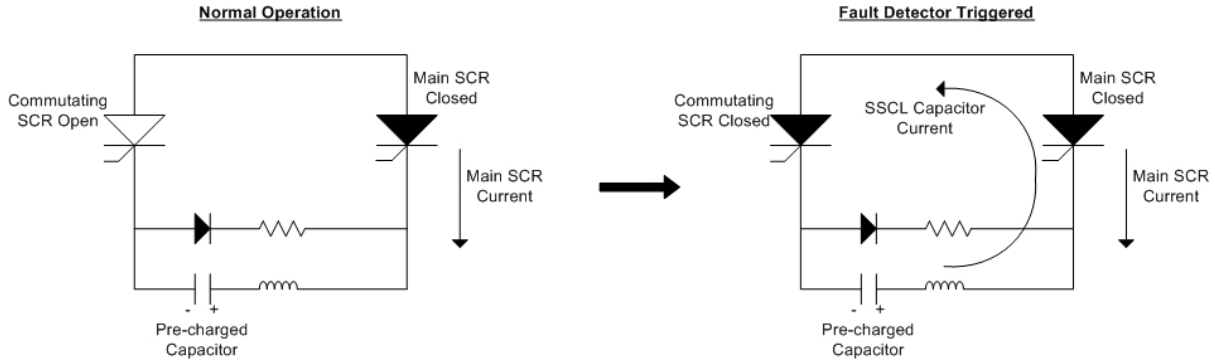


Figure 4-11
SSCL Current Interruption Process I

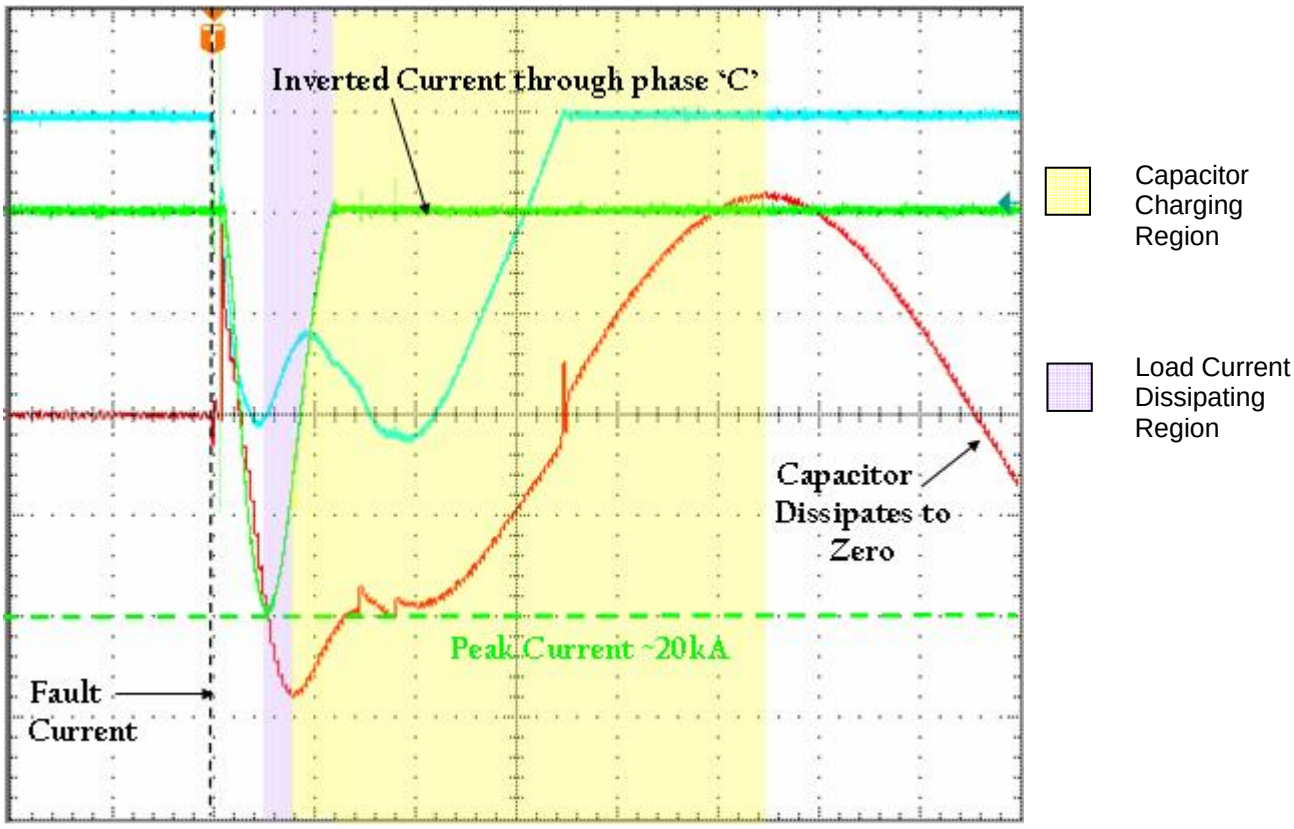


Figure 4-12
SSCL Three-Phase 63kA at 0° Fault Interruption Regions

At the instant that the current from the capacitors exceeds the current on the main SCRs, the main SCRs turn off. In Figure 4-12, the 63kA fault peaks at approximately 20kA. As the current from the capacitors surpasses the current through the main SCRs, the main SCRs open, and the remaining fault current is diverted through the commutating SCRs and it then dissipates through the resistor. The current in phase "C" eventually diminishes to zero within ~1ms and the commutating SCRs then open as well. This process can be seen in Figure 4-13. Figure 4-12 highlights the time that the fault current dissipates and when the SSCL's capacitors charge. Other fault current interruption traces can be seen in the Appendix A.

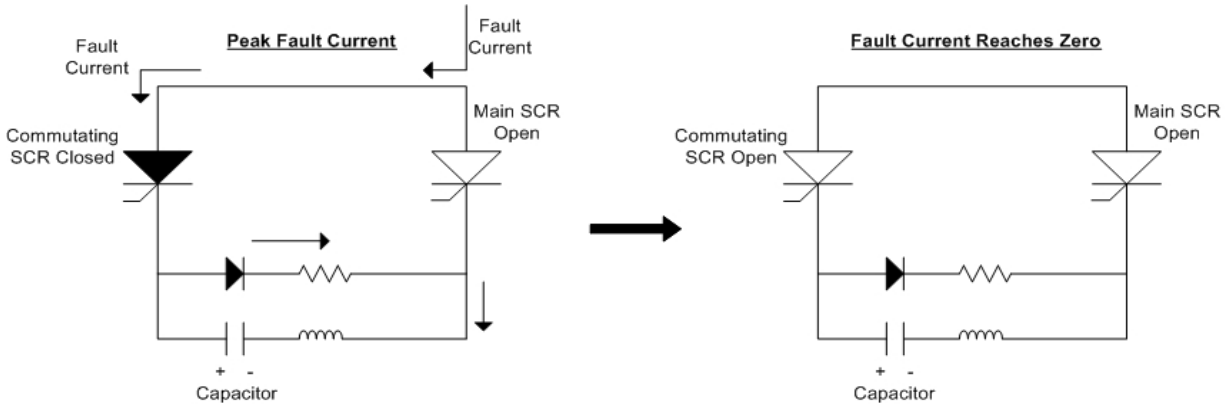


Figure 4-13
SSCL Current Interruption Process II

5
PLANS FOR 2007

Although the testing results at KEMA confirmed the Solid State Current Limiter's ability to limit fault current, there are some modifications that will have to be implemented before the limiter will be ready for field testing. The enclosure requires some modifications to allow for finalization of the racking system to engage the SSCL inside the enclosure. Furthermore, additional continuous current heat run test are required to analyze and improve the heat removal efficiency of the unit. Tests from 2005 indicated that additional improvements were needed in the continuous current heat removal system. The modified enclosure will also help ensure that the hot air created within the device is effectively exhausted out of the enclosure.

The re-closing process of the current limiter will also need to be tested in the coming months before the unit is released into the field. After the device successfully limits the fault current, the limiter will slowly phase back the main SCRs, in order to verify if the fault has cleared. The limiter's firing angle will slowly decrease and more current will be let through after it determines if the fault current has passed. The main SCRs will eventually start conducting in normal operation mode. As these features pass testing, the Solid State Current Limiter is expected to undergo one year of field testing.

A
KEMA TEST RESULTS

The following traces were other fault currents that were recorded by the oscilloscope, when the SSCL interrupted the current.

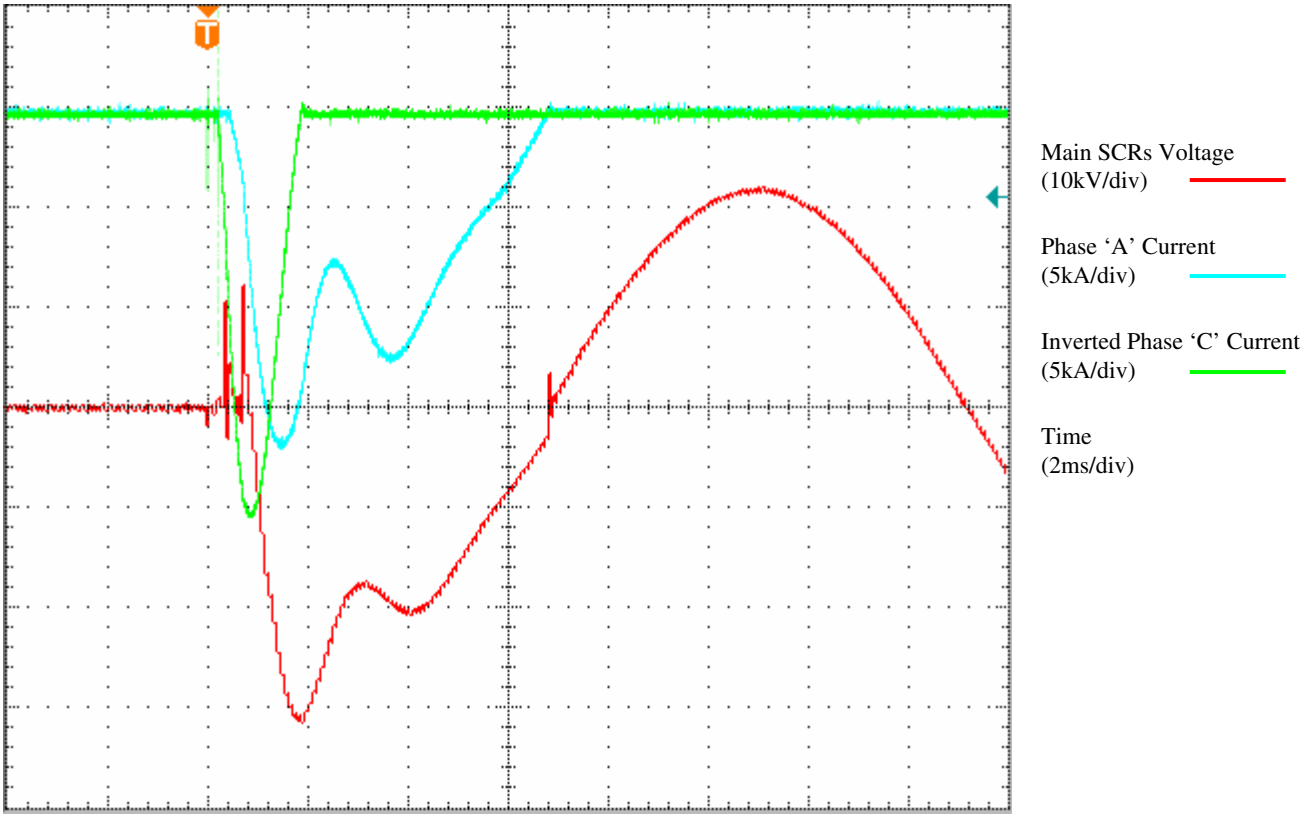


Figure A-1
63kA Three-Phase Fault at 20°

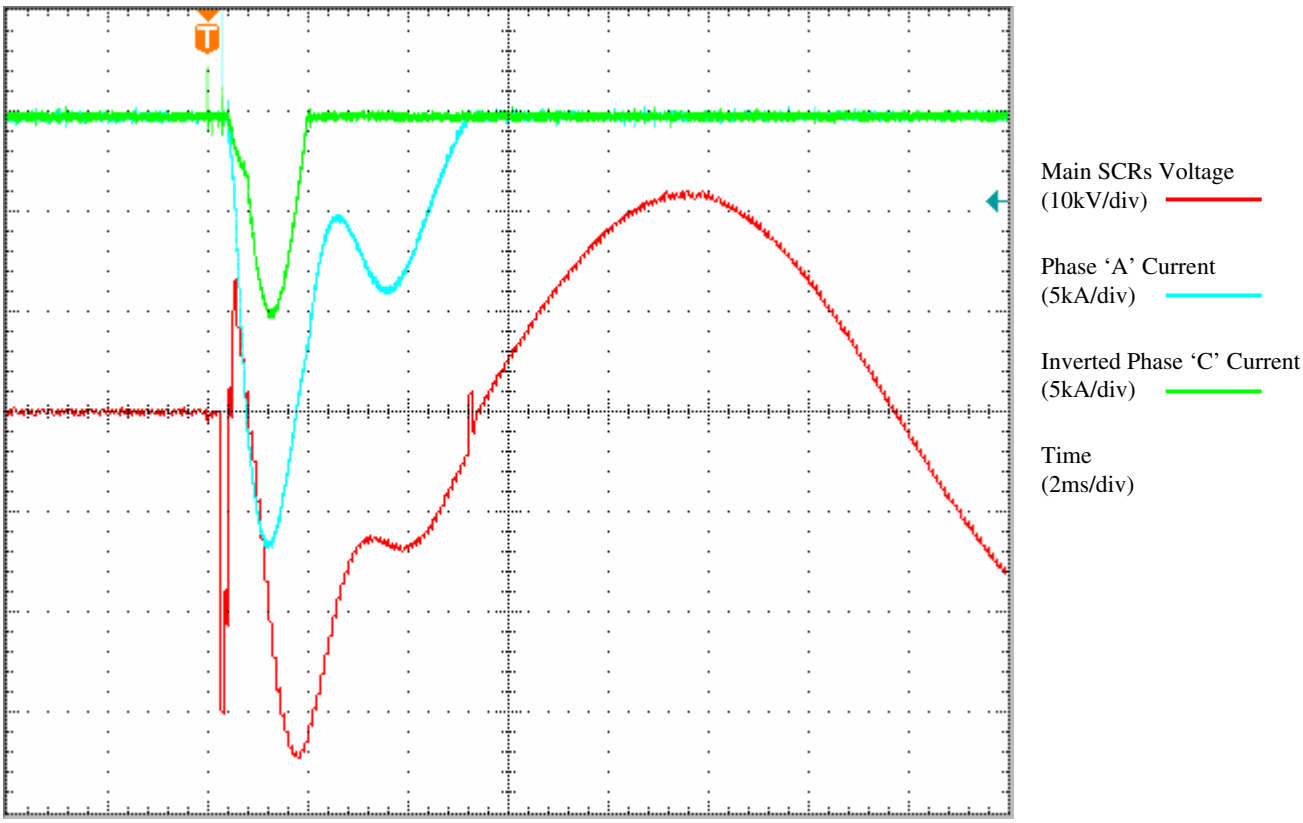


Figure A-2
63kA Three-Phase Fault at 42°

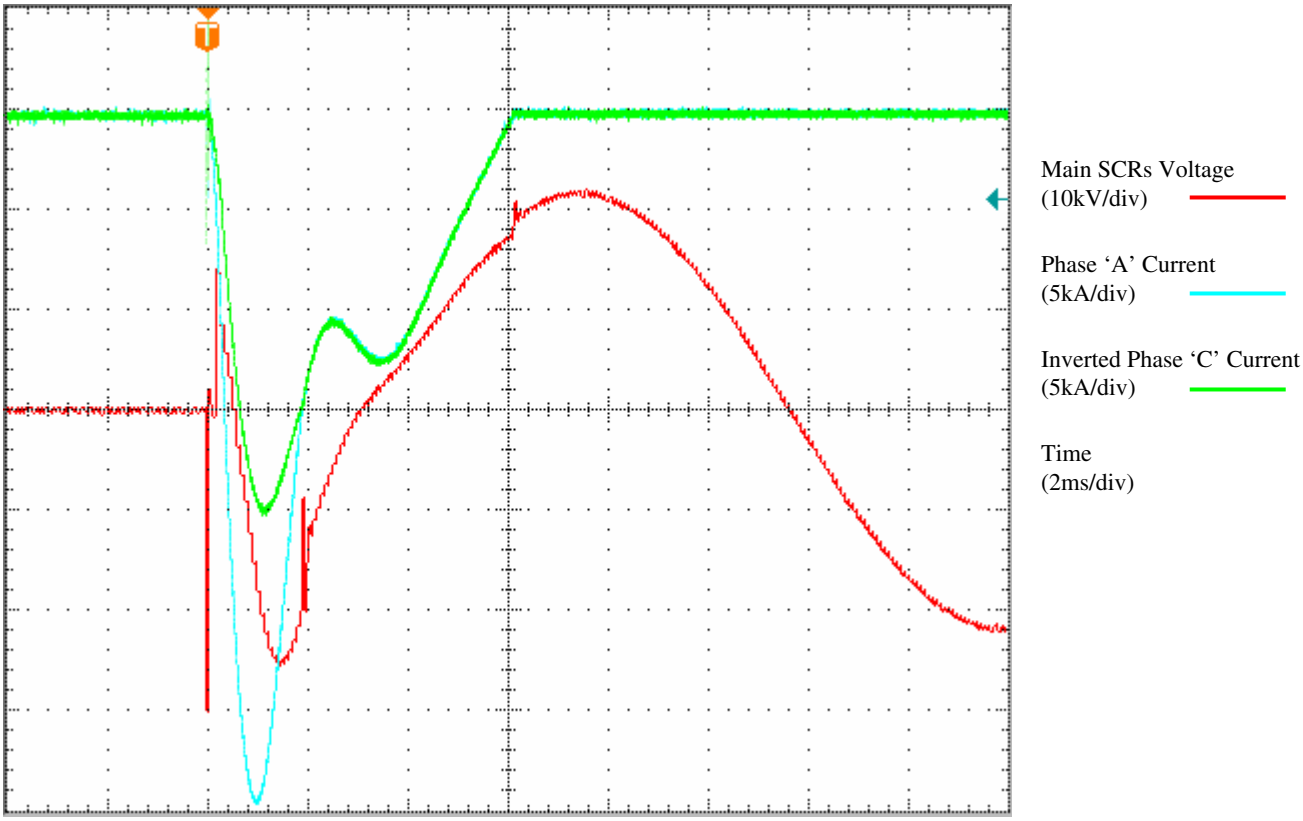


Figure A-3
63kA Three-Phase Fault at 90°

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