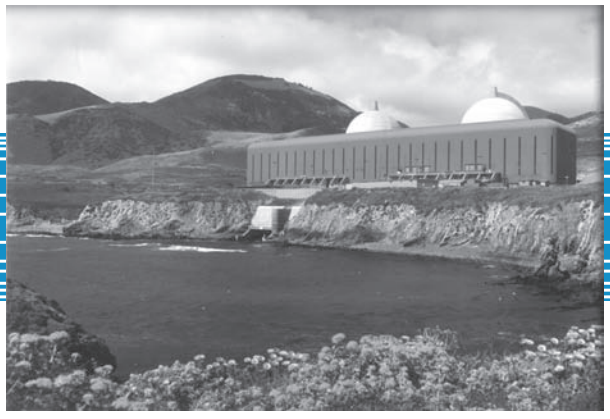
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Nuclear Maintenance Applications Center: Assessment of Printed Circuit Board Diagnostic Techniques





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Nuclear Maintenance Applications Center: Assessment of Printed Circuit Board Diagnostic Techniques. EPRI, Palo Alto, CA: 2009. 1018534.

REPORT SUMMARY

This project evaluated the techniques, theoretical methods, and recommendations made in previous EPRI reports on printed circuit boards (PCBs). The goal was to find techniques to help manage PCB life.

Background

Printed circuit boards (PCBs) at nuclear power plants (NPPs) have a wide variety of manufacturers and construction. PCBs are aging in plants, and as components age, their failure numbers increase. All NPPs have policies and maintenance programs to manage equipment performance, including PCBs. The maintenance programs differ in the importance applied to PCBs according to their relation to plant safety and operation.

Instrumentation and control (I&C) personnel are familiar with the construction and operation of PCBs but may be less familiar with board-level failure mechanisms and component failures. The Electric Power Research Institute (EPRI) undertook several investigations in an effort to develop methods of monitoring PCB performance to detect boards before failure. This project evaluated the techniques, theoretical methods, and recommendations made in previous EPRI reports, focusing on two approaches:

- Identify techniques that could be used to monitor the degradation of individual components
- Identify theoretical methods and techniques that could be developed to monitor the board and system performance

Objectives

- To assess the existing diagnostic techniques and technology used to evaluate the condition of PCBs
- To identify the capabilities and limitations of the recommended techniques and their ability both to identify precursors to board failure and to be performed on- or off-line
- To include field proof of the methods, their ease of use, cost, and availability of equipment

Approach

This project used the following approach:

1. First, an evaluation was made of previous EPRI investigations to identify proven technologies and diagnostic techniques in use in the nuclear and other industries.
2. The nature of PCB component failures was investigated.
3. Evaluation criteria were established for the selection of techniques.

4. A review of commercially available test equipment and techniques was conducted.
5. The industry was surveyed to determine which approaches and diagnostic techniques were being used for preventive maintenance programs.
6. Diagnostic techniques in other industries were investigated for the latest approaches to manage PCB life cycles.
7. Each technique was reviewed for its ability to identify failures and precursors to failure.

Results

This project produced the following results:

- PCB failures occur randomly. Some random failures are age related, so their degradation can be monitored, whereas some are unpredictable and can fail at any time. As the quality of the manufacturing processes improves, the number of unpredictable age-related failures decreases.
- Monitoring all of the failure mechanisms on a PCB is impossible. The approach taken in the military, aerospace, and automotive industries has been to identify the weak-link components and base a maintenance program on them.
- A new approach was identified for determining the time to replace a board, using the remaining life analysis, which is in extensive use in the military, aerospace, and automotive industries.
- The military, aerospace, and automotive industries are approaching this problem through a prognostics and health management program. This is used extensively on the F-22 and is finding increased use in aircraft avionics and automotive electronic systems. The ultimate goal is to have an autonomous health management computer monitor the diagnostics (out-of-specification conditions) and environmental conditions. This would eliminate the need for external testing.
- A series of proven diagnostic techniques has been recommended. These techniques are not all currently in use at nuclear plants in the United States and thus can be used to enhance a plant's preventive maintenance program for PCBs.

EPRI Perspective

The project set out to complete the work started in previous EPRI reports, with the goal of developing a set of diagnostic techniques that could be readily used to monitor PCB conditions.

Although the results of the evaluation did not yield conclusive techniques for PCB monitoring, the methods currently in use have been collected and evaluated. The problems of system- and board-level diagnostics were not designed into the current electronics, even with the new generation of electronics in use at NPPs. Board-level evaluations remain a challenge.

Keywords

Printed circuit board (PCB)
Instrumentation and control (I&C)
Diagnostics
Testing
Maintenance

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ACRONYMS

AOI	automatic optical inspection
ATE	automatic test equipment
CALCE	Center for Advanced Life Cycle Engineering
dc	direct current
EDF	Electricité de France R&D, Cedex, France
EMI	electromagnetic interference
EPROM	erasable programmable read-only memory
ESC	equivalent series capacitance
ESD	electrostatic discharge
ESR	equivalent series resistance
FAA	Federal Aviation Administration
IC	integrated circuit
JTAG	Joint Test Action Group
LED	light-emitting diode
MTBF	mean time between failures
MTTF	mean time to failure
MTTFF	mean time to first failure
MTTR	mean time to repair
NAVSEA	Naval Sea Systems Command

NiCd	nickel cadmium
NPP	nuclear power plant
PCB	printed circuit board
PM	preventive maintenance
RCM	reliability-centered maintenance
REACH	Registration, Evaluation, Authorization, and Restriction of Chemicals
RoHS	Restriction of Hazardous Substances
SAE	Society of Automotive Engineers
TAP	test access port
TDR	time domain reflectometry
UVEPROM	ultraviolet erasable programmable read-only memory

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1
INTRODUCTION

This report investigates the proven techniques and methods that are being used at nuclear power plants (NPPs) today. These techniques and methods can be adopted by plants to enhance their printed circuit board (PCB) preventive maintenance programs, with the knowledge that they have been in practice at other NPPs. In the process of identifying the proven methods that are recommended, the Electric Power Research Institute (EPRI) reports on this subject were reviewed, the industry was surveyed, and the techniques used in other industries were investigated.

An investigation of stressors, failure mechanisms, and the way boards fail was conducted to gain an understanding of the nature of PCB failures, how they occur, and the limitations of identifying failures and precursors to failure. Recommendations are made for the use of techniques and their introduction in a maintenance program.

1.1 Purpose

The purpose of the project was to identify the diagnostic techniques in use at NPPs and evaluate the condition of the PCBs for failures and precursors to failure. For proposed techniques and techniques in use, the project evaluated the ease of use of the techniques. Further, the project investigated techniques in use in other industries and evaluated whether they could be used in the nuclear industry.

1.2 Background

EPRI has previously investigated the techniques, methods, and testing to use in determining when a PCB should be replaced before it fails. Each report produced as a result of these investigations approached the situation from a different perspective. One serves as a primer to PCBs, describing how they are constructed, troubleshooting techniques, identifying failures, and refurbishing. Another investigated field failures for a variety of components found on a typical PCB. This research was carried on to a third report, which explored methods for testing individual components to understand how they aged. The final report explored diagnostic techniques and methods that could be used or developed to assess the condition of PCBs. These reports were reviewed from the perspective of identifying proven techniques usable in plants today.

1.3 Problems, Issues, and Needs

The failure of PCBs in service that cause plant trips has been a problem for a number of years, without any sign that the methods in use today have produced improvement. Some plants have programs that they consider satisfactory and have the problem under control, whereas other plants continue to have unpredictable failures. However, there are budget constraints that may limit preventive maintenance programs and thus opportunities to replace PCBs before they fail. In some cases, it is easier to replace a PCB prematurely. Run-to-failure policies can be very expensive if a failure causes an automatic scram and all of the costs associated with it.

In reviewing the practices at the plants of the respondents to the industry survey for this project, it is evident that there is not a consistent approach when it comes to PCB preventive maintenance and diagnostic techniques. Each plant has its own program and policies.

There is a need to establish, within each plant, a program or policy that reduces the overall costs of replacing PCBs while maintaining plant safety and critical operations. Therefore, there needs to be a balance between acceptable board failures (and their associated costs) and preventive maintenance program costs. This is difficult to achieve, but necessary. If a plant is not satisfied that it has achieved the proper balance, this report provides some background and options that can help them reach their goal.

1.4 Content Organization

Section 2 describes the life cycle of a PCB. It presents the typical life cycle curve and explains how the curve is not the same for all component failure mechanisms. The section on failure mechanisms includes the use of reliability data as well as degradation of performance. Failure mechanisms are affected by stressors. A cause-and-effect diagram shows the relationships among these stressors, and the text describes each one. Finally, selected failure mechanisms and how they degrade are presented in the last part of the section.

Section 3 presents information about the ways of identifying failures and precursors to failure. It begins with a section that describes the approaches that may be taken to determine when a PCB should be replaced. The plant programs should be evaluated against these options to establish a balanced program. A section is included that outlines the problems and limitations in identifying precursors to failure. This is followed by sections that describe the methods to use to locate intermittent failures and hard failures. What other industries are doing, as related to board diagnostics, is presented in the next section. Boundary scan technology and prognostics and health management (PHM) techniques used in the aerospace, military, and automotive industries are presented. The results of the industry survey are presented in the next section, which includes preventive maintenance and diagnostic techniques used. At the end of the last section is a detailed review of the four EPRI reports of previous investigations.

Section 4 presents recommendations for the evaluation of maintenance program approaches, the criteria used to recommend diagnostic techniques, and the organization of the sections covering the diagnostic techniques recommended. Section 4 further includes suggestions for selecting the diagnostic techniques to use at the system, board, and component levels. After a new diagnostic technique has been selected for use, it must be integrated into the maintenance program. The final section describes recommendations for doing that.

Section 5 contains the first of a series of recommended diagnostic techniques. The first is to perform visual inspections. Two methods are presented: manual visual inspection and thermography. Each section in the series ends with a description of the ability of the diagnostic technique methods to identify failures and precursors to failure.

Section 6 describes leakage current testing.

Section 7 includes the methods that relate to passive circuit parameter measurements. They include computer parameter monitoring, specific parameter monitoring, bed-of-nails testing, and flying probe testing.

Section 8 presents the active measurements of current and voltage. This section includes signal injection, signal tracing, bed-of-nails testing, flying probe testing, dedicated fixture testing, integrated circuit (IC) testing, computer parameter monitoring, and specific parameter monitoring methods.

Section 9 contains the list of references.

2
A PCB'S LIFE CYCLE

Failures of PCBs represent approximately 10% of the causes for plant trips. The PCBs in the power generation industry are aging due to their manufacture date and time in service. Failures of boards in critical circuits have not improved in the last seven years despite the efforts of the industry to reduce the number of in-service failures. There may be precursors to failure that would allow a board that is expected to fail to be replaced before that failure takes place. To evaluate the effectiveness of diagnostic techniques for identifying precursors to failure, it is important to understand how PCBs fail. This section describes the nature of failures, the influences that cause failures, and select failure mechanisms for the types of component found on PCBs.

Section 2.1 begins with a description of a component's life cycle, including the familiar bathtub curve, as well as studies done by the airlines and the U.S. Navy in characterizing equipment on planes and ships as they relate to failure rates as a function of service time. The results are not as expected but open the door to possibilities other than the bathtub curve. This Section also looks at the types of failure mechanisms in components and their implications to PCBs as a whole.

Stressors that influence the life expectancy of PCBs are presented in Section 2.2. All of the stressors that may be present to act on a PCB and its components are described, as well as how each stressor influences the life expectancy.

Section 2.3 lists selected failure mechanisms and causes and how they lead to failures of components on the board.

2.1 The Nature of Failures

Diagnostic techniques have been categorized as those that can identify precursors to failures and those that can identify component or PCB failures after they occur. To judge whether a particular diagnostic technique is able to identify precursors to failure or component/PCB failures, how PCBs fail must be understood.

PCB or component failure is a complex subject that has been extensively studied and researched. This section presents an overview of how PCBs and components fail, using the knowledge and insight gained as a result of research reviewed and conducted for this project.

NPPs typically use more than 10,000 PCBs in 50-plus control systems [1]. Each PCB can contain hundreds of components. The components can be discrete or integrated circuits. Integrated circuits (ICs) can contain hundreds or even thousands of subcomponents. In a critical circuit, any component on any board, and even the board itself, can fail in a manner that can

cause an undesirable condition to take place. A single component can cause the failure of the circuit or system. The following sections describe failures in components.

2.1.1 Component Life Cycle

All failures are categorized into four failure modes: open-circuit, short-circuit, functional, and degradation [1]. Open- and short-circuit failures are said to be end-state failure modes, whereas functional and degradation failures are progressive. The failures are further categorized by the time they occur in the life cycle of a component. The familiar bathtub curve shown in Figure 2-1 identifies the three regions as Infant Mortality, Normal Life, and End of Life.

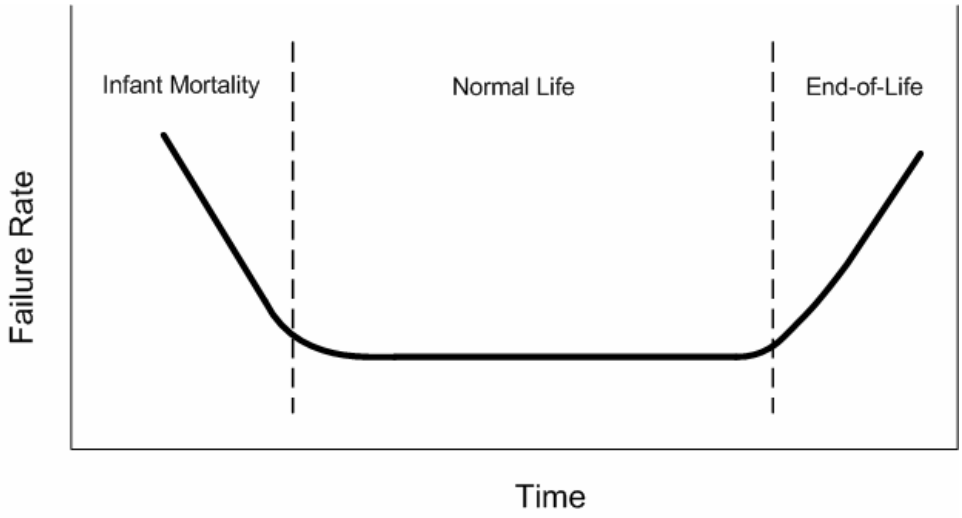


Figure 2-1
Component life cycle bathtub curve

Infant mortality failures are caused by manufacturing and material defects. Inspection, testing, and burn-in at the manufacturer generally eliminate the infant mortality failures from field units. Exceptions to this are PCB design defects and latent manufacturing and material defects that may not show up until after the board is placed in service. Failures that show up in service are considered random failures and would contribute to the constant failure rate in the Normal Life section of the bathtub curve.

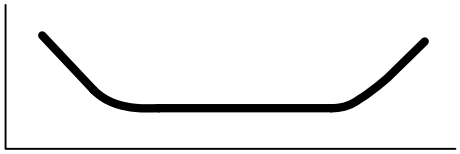
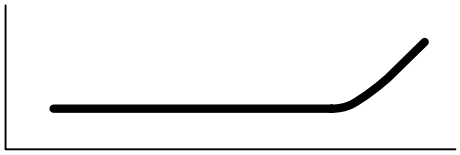
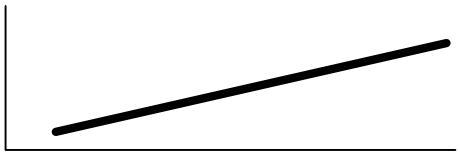
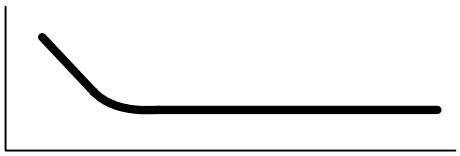
The Normal Life or random portion of the bathtub curve is shown as a constant failure rate. The failures during this part of the life cycle are not constant but rather are random due to latent manufacturing and material defect failure mechanisms. However, they are shown in this manner to facilitate reliability studies of components and circuits. A component in the Normal Life portion can fail at any time randomly with equal likelihood [2].

The End-of-Life or wear-out portion of the curve is shown as an increasing failure rate. It represents the time when a component wears out due to age-related end-of-life failure mechanisms. Failures at the end of life do not occur until a portion of time has passed, and they occur increasingly as time progresses [2].

Another aspect that must be considered is how the components operate. There are three modes of operation: on-demand, continuous, and noncontinuous. *On-demand* operation occurs when a component is not energized until the circuit it is housedin is needed to perform a specific function. An example is the plant protective system trip circuit. Failure in on-demand components is not associated with how long they are in service in operating systems but rather the number of times demands are placed on them [2]. This includes testing as well as normal circuit operation. *Continuous* operation, as the name implies, occurs when a component is in a system that is on constantly. The classic life cycle curve applies in this case. *Noncontinuous* operation occurs when a component is in a circuit that has a duty cycle and may be on for a period of time and then off. Failures for noncontinuous circuits are based on the time a circuit is on during the duty cycle or the number of times that the circuit may be switched on and off. It should be noted that some boards may have all three types of circuit operations.

Not all equipment behaves as shown in the bathtub curve. In the 1960s, when Boeing was ready to manufacture the 747, the airlines were faced with the monumental task of how to maintain the thousand of components on the plane. They undertook a study along with the U.S. Federal Aviation Administration (FAA) of the failure characteristics of components. The airlines discovered that equipment failure characteristics as a function of service time fell into six groups. The groups are explained in Table 2-1.

Table 2-1
Failure characteristic curves identified in the United Airlines (UAL) study

Group	Characteristic	Description
A		The traditional bathtub curve with an infant mortality period, a normal life period, and an end-of-life period.
B		The failure characteristic does not have an infant mortality period but rather a period of constant failure rate with an end-of-life period.
C		A constantly increasing failure rate is characteristic of the life cycle for these equipment items.
D		The equipment with this characteristic has a very low infant mortality, gradually increasing to a constant failure rate for the rest of its life cycle. It does not have a wear out or end of life.
E		Equipment with this characteristic has a constant failure rate for the service life cycle. No infant mortality or end of life is present.
F		This failure characteristic has an infant mortality and a normal life period with a constant failure rate. It does not have a wear out.

The results were not what were expected. In 1978 Nowlan and Heap published the results in a paper titled "Reliability Centered Maintenance" [3]. Subsequent studies were conducted by Brogberg, the Maintenance System (Development) Program (MSP), and Submarine Maintenance Engineering Planning and Procurement (SUBMEPP) [4, 5, 6]. The results are shown in Figure 2-2.

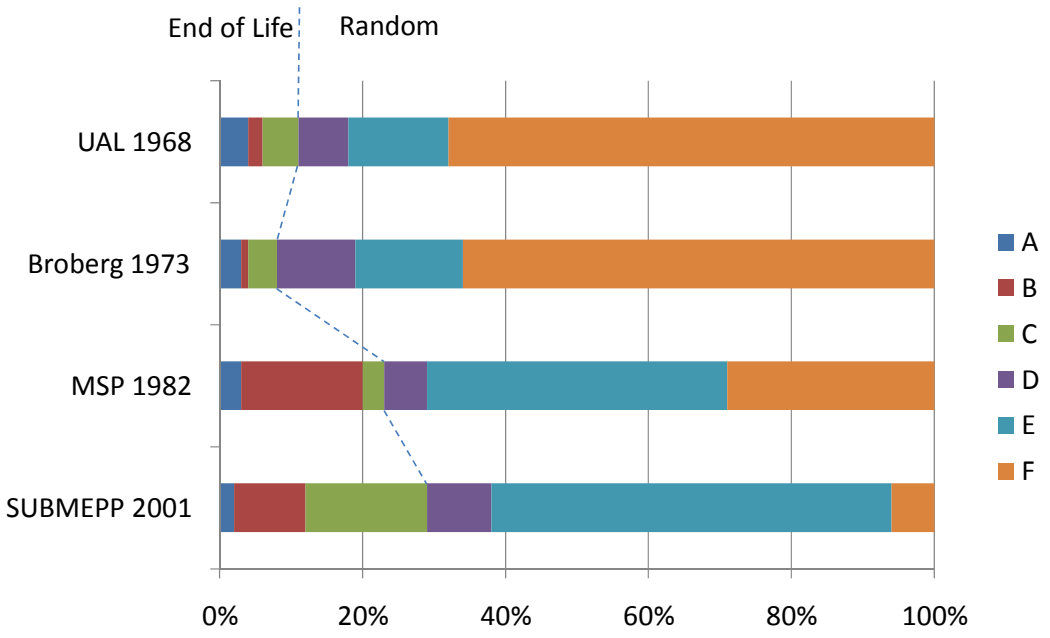


Figure 2-2
Distribution of failure characteristics

The UAL and Brogberg studies reflect the characteristics of failures on aircraft, whereas the MSP and SUBMEPP studies involved naval vessels. Groups A and B have a characteristic wear-out or end-of-life failure profile. Group C has an increasing failure rate with time, which "may be explained by the complexity of the component. The simpler the component and the fewer failure modes attributed to it, the more likely that sudden wear out occurs, if indeed there is an age and reliability relationship" [7]. Allen further stated in [7] that "these curves have been used to demonstrate the precept voiced back in 1961—that random failure predominates." Allen also noted, "Characteristic C components tended to be more complex that characteristic B. Complex components have multiple modes of failure and those individual modes may fit characteristic B when viewed in isolation. However, wear-out patterns among these individual modes tend to occur at different times and when viewed in the aggregate, the overall failure rate pattern matches characteristic C" [7]. Note that the components that were part of these studies were for all types of equipment items and may not reflect the nature of PCBs directly.

Notice in Figure 2-2 that the A, B, and C age-related end-of-life characteristics account for a small percent of the equipment. For the UAL study, it was 12%; Broberg, 8%; MSP, 23%; and SUBMEPP, 29%. Most failures were unpredictable random failures.

The results of these studies indicate that the familiar bathtub curve may not be applicable in all cases, and random failures may predominate. They further indicate that as complexity increases, the failure characteristics of equipment may increase as service time progresses. Information could not be found to demonstrate that this is the case for PCBs, but it is a possibility.

2.1.2 Component Failure Mechanisms

Each component has multiple failure mechanisms. A *failure mechanism* is the chemical, physical, or material process that leads to the component failure [1]. These three failure mechanism processes are driven by environmental, electrical, mechanical, and other stressors. (Stressors are discussed later in this report.) Failure mechanisms can be random or age-related or both.

Random failure mechanisms are normally error-induced, caused by material, manufacturing, or misuse defects. They occur without warning with equal likelihood at any time during the life of a component. MIL-HDBK-217 (Military Handbook: Reliability Prediction of Electronic Equipment) presents a catalog of parts with failure rates and the factors to be applied to adjust for changes in stressors and error-induced defects [8]. This handbook, as well as the Weibull database, Telcordia, and Bellcore have become the resources for determining the reliability of components, PCB assemblies, and systems. The handbook's intent is not to provide a method of establishing the real-world failure rate of an assembly but rather to compare the reliability of competitors in the bidding process and the effect on reliability of changes in design. It is a probabilistic approach because it views the component with a multitude of failure mechanisms as a single or lumped failure mechanism. Further, it takes the data derived from tests or the field and formulates a constant failure rate for the component. This is often called the *bottom of the bathtub* curve, where failures occur at a constant rate. This does not happen in the real world, and constant failure rates from MIL-HDBK-217 should not be taken as the true failure characteristics over the life of a component. MIL-HDBK-217 includes a baseline failure rate that is modified by environmental, quality, and electrical stress factors. The exact factors vary with the part type. The failure rate data have been used to derive two familiar terms: mean time to failure (MTTF) and mean time between failures (MTBF).

MTTF is the time to failure of a nonrepairable component or system. It is equivalent to the mean of its failure time distribution. Because this a nonrepairable component, MTTF is sometimes thought of as the mean time to first failure (MTTFF). The MTTF is related to the failure rate by:

$$MTTF = \frac{1}{\lambda} \qquad \textbf{Eq. 2-1}$$

Where λ = the failure rate.

The probability that a single component from a large population of the same components will survive to a particular time can be represented by Equation 2-2.

$$R(t) = e^{-\lambda t} \qquad \textbf{Eq. 2-2}$$

Given that $\lambda = \frac{1}{MTTF}$, the probability expression can be written as

$$R(t) = e^{-\frac{t}{MTTF}} \qquad \textbf{Eq. 2-3}$$

When t = MTTF, $R(t)$ = 36.8%.

When t = 0.05 MTTF, $R(t)$ = 95.1%, meaning that there is a 95% probability that a component will survive to 0.05 MTTF.

MTBF usually applies to repairable systems and includes a new term called *mean time to repair* (MTTR). MTBF is the sum of MTTF and MTTR. Because the system is repairable and continues to function after the repair has been completed, MTBF represents the successive time between failures and repair times. If the repair time is small in comparison to the time between failures, the value of MTBF approaches MTTF, and the terms have been used interchangeably. This can be a source of great confusion if not clearly understood.

Age-related end-of-life failures generally have a long period of no failures and an increased failure rate as the component wears out. The wear out is a basic failure mechanism of the component and not related to error-induced defects. Age-related failures may be predictable if the predominant age-related failure mechanism is measurable. The predominant age-related failure mechanism behaves in a manner similar to that shown in Figure 2-3.

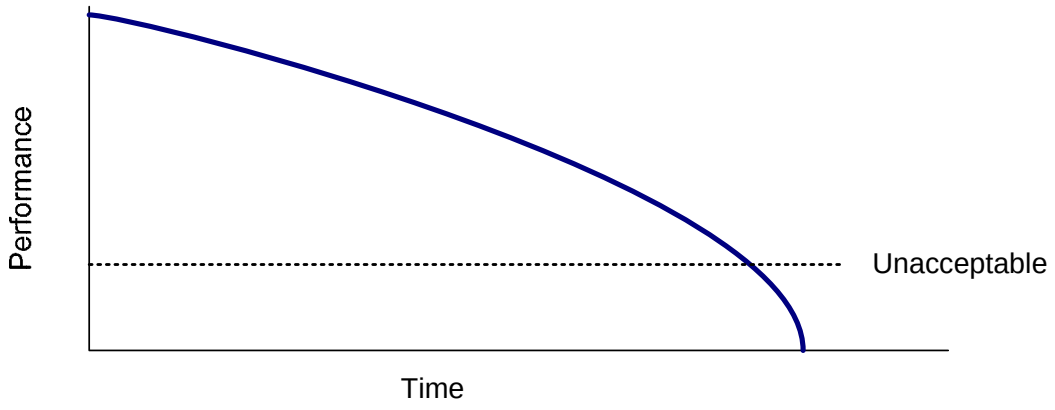


Figure 2-3
Age-related failure mechanism degradation

The age-related failure mechanism begins at an as-new performance level when an aging stressor is applied. The age-related failure mechanism is associated with a parameter performance indicator that degrades as time progresses. As the degradation of performance continues, a point will be reached where the performance is not acceptable. If allowed to continue to age, the component would fail to an end state. In some cases, the point at which performance is unacceptable is not reached until the component fails.

Several models have been used to describe the aging process. The Arrhenius model is the most familiar, but it is not the only one, and it does not provide an accurate result when two or more chemical reactions are involved [9]. Another aging model is the Eyring model, which can accommodate a second stress in addition to temperature. Yet another is the Inverse Power model,

which can be applied to dielectric breakdown in capacitors and aging in multicomponent systems [9]. There are others, but the point is that age-related failure mechanisms do not all age in the same way. These models use acceleration factors, which allow testing at a higher level of the stressor for a shorter time to be applied to the operational situation. When selecting the acceleration factors and methods of accelerated aging, care must be taken to identify the correct predominant failure mechanism and its associated aging model. Temperature alone may not provide accurate data for the component's life expectancy.

The final situation is when there is a combination of both age-related failure mechanisms and random failure mechanisms. There are cases where stressors can act on error-induced defects that cause them to be age-related. If the defect is significant enough, the failure can occur anytime. However, if the defect is just significant enough to start an aging process in the presence of an aging stressor, the failure will not occur until the defect ages, and the defect or results of the defect grow, causing failure.

In addition to random failures due to the error-inducted defects, age-related error defects can be thought of as being normally distributed. As time progresses and the stressor causes chemical, mechanical, or physical aging to occur at the defect site, a point will be reached when the defect will cause failure. The failures will also have a distribution with time. If this type of failure mechanism is viewed as part of the random data, the time at which failure occurs is also considered random, and all of the failures that occur in a large population are lumped together as one failure rate.

It should be noted that higher quality components will have lower random failure rates. As the quality of the components goes down to the commercial grade level, latent manufacturing and material defects will play an increasing role in determining the type of failure that occurs. The lower the quality, the more predominant unpredictable random failures become. The higher the quality, the fewer the number of latent defects and the more likely the failure could occur due to a normal age-related failure mechanism.

Thus far, failure mechanisms have been viewed from a probabilistic perspective as a component with a multitude of failure mechanisms lumped together to result in a constant failure rate. A more accurate methodology is a deterministic approach in which individual failure mechanism types are looked at for their reliability or failure characteristics. The on-line statistics handbook *NIST/SEMATECH e-Handbook of Statistical Methods* [10] identifies this as the *competing risk model* and likens the process to a race in which all of the failure mechanisms are competing to see which one can reach failure first. It is assumed that each failure mechanism is independent of the other and that the life distribution is known. They are all going as fast as they can and not aware of the other failure mechanisms. The first to reach failure wins the race, and the component fails. This is sometimes called the *physics of failure method,* and a number of companies offer database information and programs to review PCB design from this perspective. Using this approach can help to determine the predominant failure mechanism, which we will see in Section 3.2 is necessary to establish a means of condition monitoring.

Figure 2-4 shows a depiction of 10 components of the same part type. The assumption is that they all start service with an equal level of performance. During normal life, the components fail randomly at 6, 9, 11, 16, and 18 years. The failure rates in MIL-HDBK-217 are based on these components and are calculated as a constant failure rate. These failures are due to latent defects

that are acted upon by stressors, causing the parameter that can be measured to degrade in time. One component that fails at 11 years, however, fails suddenly without perceivable degradation. This may be because the degradation is not one that can be measured, or it may be a catastrophic failure that gives no warning. All failures in the normal life cycle are random, unpredictable failures. The last five components fail as a result of normal aging of a fundamental failure mechanism. They fail at 20, 22, 23.5, 24.3, and 25 years. Their failure is predictable, and the failure rate increases with time.

Failures can also differ from plant to plant due to differences in design and maintenance programs [2]. When a critical PCB fails in service and causes a trip, a root cause analysis is normally performed. Based on the results of the analysis, a corrective action is established and performed as part of the maintenance program. The failure rate of the mechanism that caused that failure is changed as a result of the corrective action. For example, when tin whiskers caused the failure of a critical digital logic board at Millstone on April 17, 2005, the corrective action at a number of plants was periodic inspection or brushing the boards to remove the whiskers. The corrective action would essentially eliminate the failure mechanism; thus the failure rate was changed. Preventive maintenance (PM) activity focused on reducing the stressor acting on a particular failure mechanism will also reduce the overall component's failure rate.

Take this situation and translate it into the number and different types of components found on a PCB, then take that and compound it with the number of boards in a circuit, and you will have some idea of the complexity of the situation.

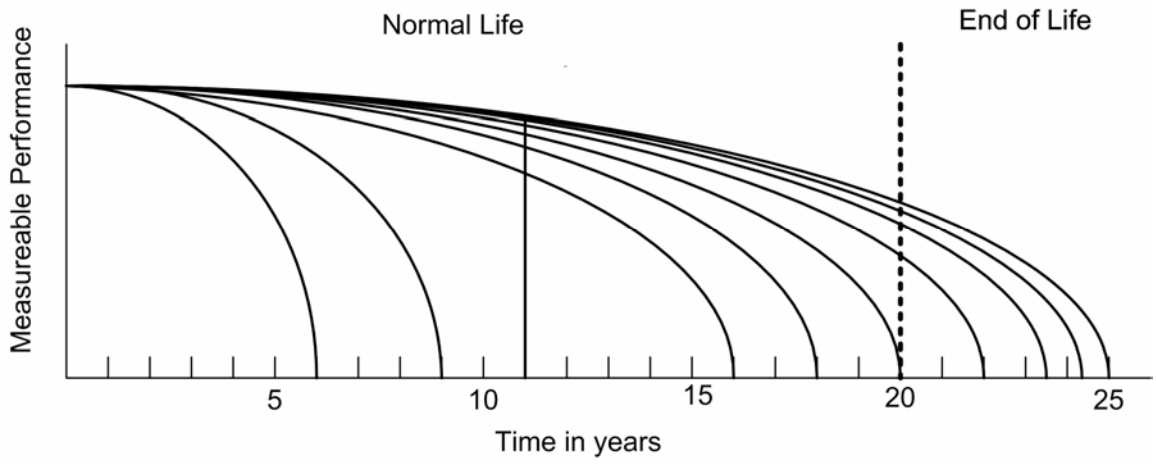


Figure 2-4
Failure characteristics of 10 components

2.2 Stressors That Influence the Life Expectancy of PCBs

The number of years that a PCB will last before it fails is influenced by many stressors. The quality of the board, its components, and the workmanship of manufacture will greatly affect how long the board will remain functional. The board's design, which determines the levels of electrical stress to which the individual components will be subjected, has an effect on board life. The environment in which a board operates can either decrease or increase its life dramatically. How boards are handled and stored can be a factor in their life expectancy. Mechanical and chemical stressors also affect a board's performance and service life. Failures caused by failure mechanisms that are influenced by all of the above stressors can be decreased by reducing the stressors that affect the time to failure of components on PCBs. This section provides information about these stressors. Figure 2-5 shows the relationship of the stressors that influence a PCB's life expectancy.

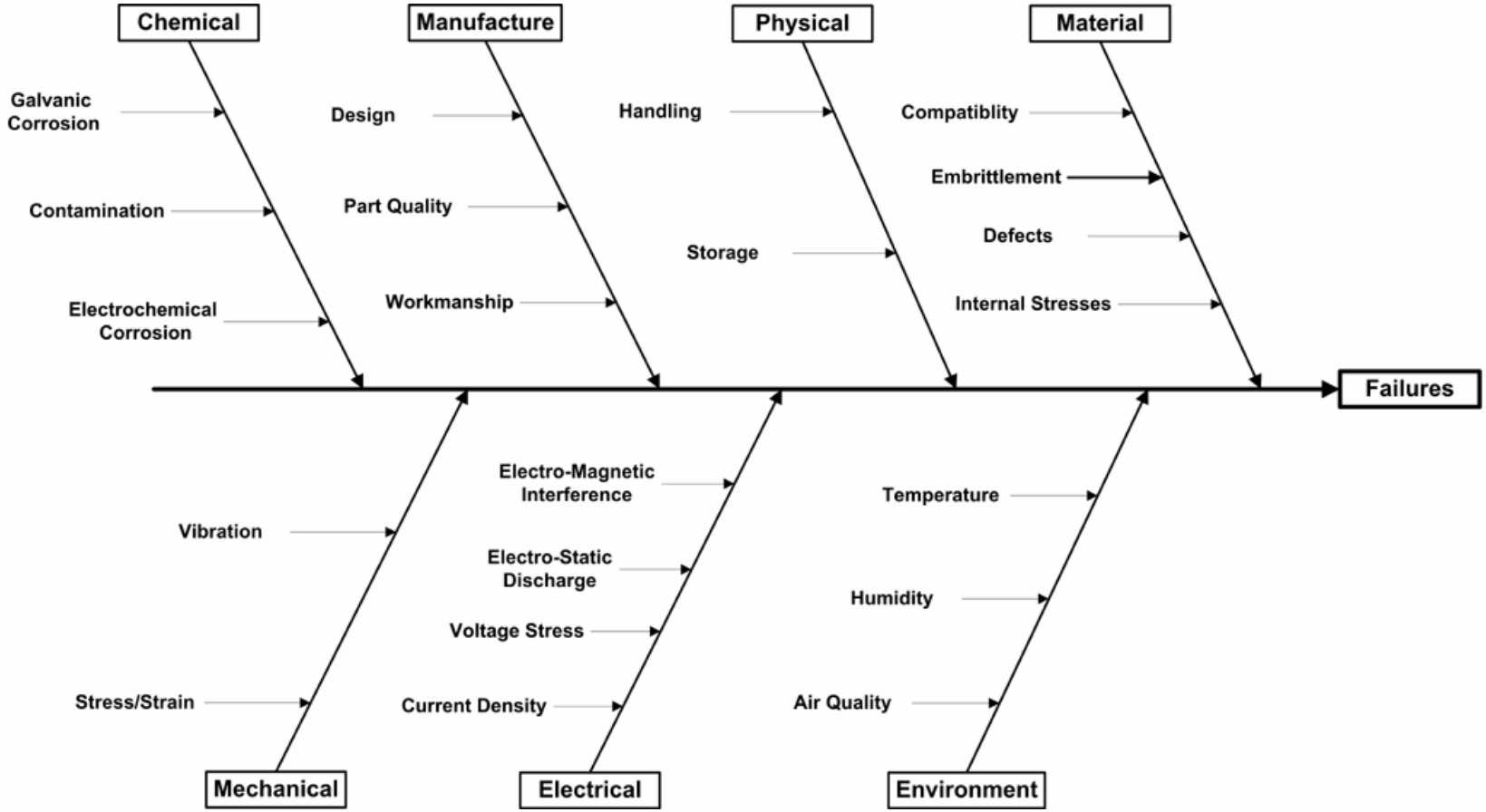


Figure 2-5
Stressors that influence PCB life expectancy

2.2.1 Manufacture

2.2.1.1 Part Quality

The quality of the PCB is one of the important items that can enhance the life expectancy of a PCB. The use of the highest quality military specification parts can add many years to a component's longevity. For example, MIL-HDBK-217F uses a quality factor (π_Q) in the equation to predict failure rates [8]. A unijunction transistor manufactured to MIL-S-19500 with a quality level of JANTXV has a factor of 0.7, whereas one manufactured to JAN quality level (lower quality) has a factor of 2.4. In other words, the lower quality transistor has a failure rate 3.4 times that of the higher quality transistor. Buying the best military specification components is more expensive, but the increase in reliability is worth it for operations that are critical or important to safety circuits.

Legacy PCBs may not use the best quality parts and, therefore, those parts can fail before higher quality parts. Even though nothing can be done as long as these components are in service, when they are replaced or refurbished, the best parts should be used.

2.2.1.2 Workmanship

Using the best components is only one part of the process. Just as important is how well the PCB is manufactured. Newly assembled, repaired, or refurbished PCBs should be produced to meet the acceptance requirement of IPC-A-610D, *Acceptability of Electronic Assemblies* [11]. The report covers the attachment of components to PCBs, dressing the cables properly, and connector installation. The manual includes pictures and drawings not only of acceptable items but also defects.

2.2.1.3 Design

The design of PCBs can reduce their reliability and life expectancy if not properly done. Each manufacturer has its own procedures and experience for designing PCBs. The tolerances they use as well as board layout play a part in the reliability of the board. If heat-generating components do not have sufficient clearances with the board or other components, they can overheat, which will raise their internal temperatures and thus decrease their life. In power supplies, if components are not selected properly, they can be overstressed electrically and fail prematurely. Parts that are selected for carrying currents may be underrated, and thus overheating can occur. If shielding and ground planes or traces are not designed properly, the components can be subjected to unwanted electromagnetic interference (EMI), which can cause overstress and failure. Relays that are underrated and energized continuously in fail-safe circuits can overheat, resulting in coil failure. However, if the design is too conservative, there can be problems with oxide buildup on relay contacts that depend on the wiping action of the make/break arc to remove the buildup. All of these stressors can influence the life expectancy of PCBs.

2.2.2 Materials

2.2.2.1 Compatibility

The formation of intermetallic compounds and thermomechanical stresses due to differences in thermal expansion are two factors that influence the life of components on PCBs. "Two different metals [in contact with each other tend to] diffuse into each other creating a species materials which are combinations of the two materials" [12]. Such is the case between gold and aluminum, which form five compounds, one of which is $AuAl_2$ or "purple plague" [12]. This can create formation voids, the rate of which depends on temperature. The continued void formation ("Kirkendall voids") leads to increased resistance and ultimately failure of the connection between the gold wire and an aluminum pad [12].

Materials with a large difference in thermal expansion can cause stresses at the joint between them due to thermal cycling. Such can be the case between solder and the substrate material of a PCB. Continued thermal cycling can cause microcracks to form, gradually increasing resistance of the connection and evolving into cracks great enough for the connection to be broken.

2.2.2.2 Embrittlement

Embrittlement occurs differently in metal than in organic materials. In metals, embrittlement occurs gradually due to stress cycling, which can be a result of temperature changes. The first stage of embrittlement is the formation of slip bands at metal dislocations that nucleate short cracks. As the metal is continually stressed and relaxed, the short cracks grow until the metal fails.

Organic materials become brittle by a cross-linking process. Molecules of organic materials and mixtures of materials are very long. During the manufacturing process, the materials are mixed with plasticizers or through vulcanization that act as a catalyst promoting connections between the molecules. The compound that results in a molded or extruded plastic or rubber is flexible, can be stretched (elongation), and has strength (tensile). For example, as the insulation on ribbon cable continues to age, it continues to cross-link. In some forms of the insulation, the properties will continue to improve, but eventually they will deteriorate. The insulation becomes less flexible, and gradually cracks form as the molecular chains are broken due to stress. The cracks continue until the insulation is cracked through to the conductor, and ultimately the cable conductor will fail.

2.2.2.3 Defects

Material defects such as impurities, inclusions, crystalline formation, voids, and cracks contribute to reducing the life of a component on a PCB. Impurities that are destructive can accelerate cracking and intergranular compound formation. They can affect the physical properties of the material as well as the electrical properties. Inclusions are generally associated with minerals but can be any other material trapped inside the mineral during its formation. Like impurities, inclusions can have an adverse effect on the physical and electrical properties of materials. Crystalline formations take place over time in an amorphous material, causing a

change in physical and electrical properties. Voids are introduced during the mixing or preparation stage of the processing of materials into molds or through an extrusion process. Voids reduce the strength and electrical properties of materials. In time, through thermal cycling, the gas within the voids can expand and contract, thus adding stress at the void/material interface and causing microcracking to occur. Voids in gold plating increase the porosity of the gold, which can expose the copper substrate and cause corrosion. In some cases, partial discharge (corona) can occur in voids where the dielectric stress exceeds the breakdown voltage of the gas, usually air.

2.2.2.4 Internal Stresses

Internal compressive stresses can cause the growth of crystalline structures in the form of tiny hairlike structures (*whiskers*) from the surface of elemental metals. This has been known to occur in tin, zinc, silver, and gold. The cause of whiskering is not well-known, but it appears to be promoted by the mechanical compressive stresses that occur during electroplating, diffusion of different metals, and thermal cycling. The formation of whiskers does not appear to be the result of an electromagnetic field. The whiskers grow over time but seem to be accelerated by temperature. Tin whiskers have been a problem in the nuclear industry since the increased use of lead-free solder.

2.2.3 Physical

Handling and storage also play a large role in the life expectancy of PCBs. EPRI report 1007916, *Printed Circuit Board Maintenance, Repair, and Testing Guide,* provides a comprehensive discussion of the proper storage and handling of PCBs [1]. This report should be followed in order to avoid damaging the board, thus increasing its life expectancy.

2.2.3.1 Handling

Improper handling of PCBs and their components can cause damage that can lead to a failure. Electrostatic discharge (ESD) from static electricity on a person's body can cause dielectric failure due to open or short circuits in sensitive components. Not paying attention to the use of shielding material to prevent ESD and not properly grounding when handling a PCB are two causes of board failure. Stacking one board on another or placing objects, such as tools, on boards can crack, bend, and scratch components, which in turn can lead to failures. Touching conductive surface with bare hands can leave oils that promote corrosion, which can cause failures. Removing boards from backplane connectors too frequently can cause wear on the connectors that results in intermittent open circuits. Placing too much pressure or stress on switches and keyboards can cause internal breakage and ultimate failures. A good rule: handle PCBs only when necessary and as little as possible.

2.2.3.2 Storage

Improper storage can cause damage due to contamination, physical damage, corrosion, and board component deterioration. Storing PCBs in areas without environmental controls can lead to the formation of condensation and corrosion. Not placing the boards in sealed antistatic bags can lead to ESD conditions and contamination from dust and dirt settling on the surface. Physically stacking boards on one another can damage the connectors and components on the boards. These stressors can lead to failure.

2.2.4 Chemical

2.2.4.1 Electrochemical Corrosion

Electrochemical corrosion is the breaking down of a material by means of a chemical reaction due to another chemical or oxygen and water. Corrosion such as rust can occur on an iron surface in contact with moisture in the air. Corrosion can form on PCBs in the presence of a chemical such as an electrolyte from a battery or a capacitor. The base material gradually gives up electrons to the positively charged ions of the electrolyte. Over time, this will cause pitting in the base material. If this occurs in a conductive path, the resistance can increase, and eventually the conductive path will be broken, resulting in an open circuit failure.

2.2.4.2 Galvanic Corrosion

Galvanic corrosion occurs when two metals are in contact with each other in the presence of an electrolyte. An electrically conductive path is needed to form a galvanic couple, where the more noble metal corrodes at a slower rate than the less noble metal.

2.2.4.3 Contamination

PCBs and their components can be contaminated by body oils; dirt and dust; liquids; cleaning solvents; and pollutants in the air such as smoke, nitrous oxide, and ozone. Contamination can form low-resistance paths on the surface of PCBs and combine with electrolytes to cause electrochemical corrosion. In time, this can lead to short circuits.

2.2.5 Environment

The environment in which the PCB operates also has a great effect on the longevity of the board. There are three primary stressors that are described in the following sections: temperature, humidity, and air quality. These influence PCB life expectancy more than other environmental conditions.

2.2.5.1 Temperature

A component's temperature can change the failure rate dramatically. The 10°C rule generally applies to components found on a PCB. The rule states that for every 10°C rise in temperature, the failure rate doubles. MIL-HDBK-217 modifies this from the experience in the field and through testing. A component's temperature may be dictated by its design, but the temperature in a cabinet or module can influence the life of the components on a board. Placing cabinets in hot locations or not having adequate air flow within the cabinet can reduce the board life. It is important to keep air filters in cabinets clean, to ensure that there is adequate air flow; in some cases, even cooling the cabinet's internals can help reduce failure rates.

2.2.5.2 Humidity

Humidity plays a role in the life of a PCB only if it is too high. Low humidity will inhibit corrosion. High humidity will promote corrosion and can cause conductive paths to form between traces, especially in the presence of contaminants such as dust. If the boards are in a high humidity area and the failure rates are high, dehumidifying the atmosphere within the cabinet can help to prevent corrosion. Conformal coatings can also prevent moisture-induced failures.

2.2.5.3 Air Quality

Air quality can play a role in the life expectancy of a PCB. Boards that are located in areas where they may be exposed to salt-air or chemicals are susceptible to chemical reactions occurring on the surface of boards. Salt-air can also leave salt deposits on board surfaces that in the presence of humidity can cause short circuits or low-resistance paths to form.

2.2.6 Electrical

Electrical stressors can cause premature failures to occur in PCB components. There are several electrical stressors that are of interest: ESD, voltage stresses, EMI, and current density. Each of these stressors can cause an abnormal event to occur within components that can either cause immediate failure or begin an age-related failure mechanism.

2.2.6.1 ESD

ESD is caused by personnel with a buildup of static electricity touching a conductive surface on a PCB. A static electrical potential can build up when two materials are rubbed together. This is known as *tribocharging,* and a large potential can be developed. When two objects of different potential come in contact, an electrostatic current will flow and can cause damage to electronic components. The discharge does not have to be accompanied by a spark to cause damage. A voltage difference of only 12 volts can cause damage in a component that may not show up for years. Care must be taken when touching any conductive surface of PCBs or any conductive paths connected to PCBs.

2.2.6.2 Voltage Stress

Voltage stress across a dielectric material either between conductors or from a conductor to ground can, over time, cause a dielectric failure (breakdown). If the voltage stresses are too high or if impurities and voids exist in the dielectric, stresses can build up and cause dielectric breakdown.

2.2.6.3 EMI

EMI is generally caused by cabling from another system with a high inductive load being too close to conductors for the circuits on the PCB. The coupling of the circuits to the inductive load and the PCB wiring can cause an induced voltage transient in the PCB. The voltage transient in the board can overstress components and cause immediate failure or can cause a breakdown in part of the dielectric material, thus promoting the propagation of dielectric breakdown.

2.2.6.4 Current Density

The current in a conductive path causes the conductive material to heat. If the current density is too high, the heating can become excessive and cause the temperature of the component to increase and eventually fail prematurely. Current density can increase due to a reduction of the conductive path by corrosion or electrochemical migration.

2.2.7 Mechanical

Mechanical stressors such as vibration and stress or strain can cause components and connections to fail by fatigue.

2.2.7.1 Vibration

Although, in most cases, vibration may not be a factor that influences the life of a PCB, there may be some applications where the vibration of pumps or other equipment may induce vibration in a board. Vibration causes the boards to flex, placing stress on the connections, particularly the connectors and terminal blocks. They, in turn, can cause parts to loosen, thus causing intermittent failures and metal parts to fail in fatigue.

2.2.7.2 Stress or Strain

Stress or strain can be caused by vibration, mishandling, or improper installation. Placing a stress or strain on a board, component, or connection can cause microcracks to form that in time will grow into larger cracks. Eventually the board, component, or connection will fail in fatigue.

2.3 Failure Mechanisms

There are literally hundreds of failure mechanisms for PCBs and their components. EPRI report NP-1558, *A Review of Equipment Aging Theory and Technology,* includes a list of failure mechanisms in Appendix D, many of which are described in detail in the body of the report [9]. It is not the purpose of this report to list and describe all of the failure mechanisms that apply to PCBs but rather to describe selected and newer failure mechanisms. Table 2-2 contains a selection of important failure mechanisms in alphabetic order.

Table 2-2
Selection of failure mechanisms

Anode gold evaporation	This failure mechanism is found in electronic tubes and refers to the gradual eroding of the gold on the tube's anode. Anodes are normally gold-plated. In the operation of the electron tube, the anode is positively charged, and electrons from the cathode are attracted to it. The electrons have kinetic energy and mass as they travel from the cathode to the anode. When they strike the anode, they dislodge atoms of gold from the surface of the anode and produce heat. The surface can become hot enough to evaporate the gold. The gold vapor cools into droplets, which can deposit on the cathode and will diminish the electron production from the cathode, or they can settle on insulating surfaces and will eventually cause arcing.
Ceramic cracking	This failure mechanism occurs in ceramic capacitors. The capacitors are constructed by layering ceramic sheets between metallized electrodes. Ceramic is brittle and has low strength in tension and high strength in compression. Cracks in the ceramic can occur due to mechanical vibration and shock, or they can occur from thermal shocks during soldering or due to proximity to an overheated component on the PCB. Cracks lead to a decrease in insulation resistance and possibly short circuits.
Connection failure (internal)	Any electronic package that has an internal wire bonded to the electronic components can exhibit this failure mechanism. These components can include capacitors or ICs. The lead failures can occur due to a number of causes. Corrosion, contamination, and thermal cycling that overstress and fatigue the leads or the bonds are the primary causes. This results in an open circuit.
Contamination	Contamination is a failure mechanism that can occur during manufacture or operation. During manufacture, contamination can be built into the component, or it can be caused by an external event, such as plating salts not completely removed from the part or PCB. During operation, contamination can be the result of improper storage or handling as well as the environment.

Table 2-2 (continued)
Selection of failure mechanisms

Corrosion	There are two types of corrosion of interest: electrochemical corrosion and galvanic corrosion. Electrochemical corrosion is the breaking down of a material by means of a chemical reaction due to another chemical or oxygen and water. Corrosion such as rust can occur on an iron surface in contact with moisture in the air. Corrosion can form on PCBs in the presence of a chemical such as an electrolyte from a battery or a capacitor. The base material gradually gives up electrons to the positively charged ions of the electrolyte. The base material is considered the anode, and the atmosphere or another area of the base metal is the cathode. A flow of electrons from the anode to the cathode in the presence of an electrolyte causes the gradual removal of the base metal and the disposition of the base metal in the electrolyte or on the surface of the cathode potion of the base metal. Anodes corrode; cathodes do not. Over time, this will cause pitting in the base material. If this occurs in a conductive path, the resistance can increase, and the location can heat; eventually the conductive path will be broken, resulting in an open circuit failure. Galvanic corrosion occurs when two metals are in contact with each other in the presence of an electrolyte. An electrically conductive path is needed to form a galvanic couple, where the more noble metal corrodes at a slower rate than the less noble metal. Metals have a standard electrode potential and can be arranged in a list generally called a *galvanic series*. The greater the difference between the standard electrode potential of two metals in contact with each other, the greater will be the rate of galvanic corrosion.
Dielectric breakdown	Dielectric breakdown is caused by the gradual development of electrical trees. Trees form as a result of voltage stresses on impurities, gas voids, mechanical defects, or conducting projections in the dielectric material. In a pure dielectric without any of the causes of treeing, the voltage is distributed either linearly (direct current [dc] voltage) or exponentially (alternating current [ac] voltage) across the dielectric. If impurities are present and the voltage gradient between impurities is high enough, the dielectric material between the impurities will break down, causing a conductive path to form. This increases the voltage stress on the rest of the dielectric. If gas voids are present and the voltage gradient across the void is high enough, the gas will break down, ionizing the gas and causing destruction of the walls of the void. Mechanical defects such as microcracks within the dielectric can cause breakdown of the surface of the microcrack. Projections from conducting surfaces into the dielectric increase the stress gradient at the projection, which can promote one of the other destructive characteristics to form. Over time, these connect with each other in what appears to be branches of a tree. This will continue until there is not sufficient dielectric to support the voltage between the electrodes.

Table 2-2 (continued)
Selection of failure mechanisms

Electrochemical migration	Electrochemical migration can occur on the surface or in the insulation of PCBs due to a conducting anode filament (in the insulation) and dendritic growth (on the surface of insulation). When a potential exists between two conductive paths or between two pins that are in contact with an insulating surface, ions will migrate between the anode and the cathode conductors. "Dendrite growth occurs as a result of metal ions going into solution at the anode and plating out at the cathode, growing in needle- or tree-like formations" [13]. "The [*conductive anodic*] filament, a copper salt, grows from the anode toward the cathode along the epoxy/glass interface" [14].
Hot carriers	Hot carriers cause electron or hole traps to form in semiconductors, increasing leakage current and shifts in the threshold voltage and leading to instability and failure. Hot carriers are either electrons or holes that have excessive kinetic energy and migrate from the location where they should reside to some other location, thus leaving an electron or hole trap.
Intermetallic degradation	Intermetallic degradation occurs at the interface between two dissimilar metals where a third compound is formed by the two metals. This happens, for example, between aluminum and gold. If the compound that is formed is a nonconductor, an open circuit can eventually occur.
Ionic migration	Ionic migration occurs between an anode and cathode at low voltage gradients in the presence of moisture. Positively charged ions migrate over the path of least resistance from the anode to the cathode. The current density in the path is high enough to cause heating, which in turn causes carbonization. This continues until the resistance of the conductive path is low enough for a flashover, and a short circuit forms [12].
Oxide deterioration	Oxide deterioration occurs in aluminum electrolytic capacitors. These capacitors are constructed in a wrapped sandwich configuration. The sandwich consists of an anode aluminum foil with an oxide layer, a paper separator impregnated with an electrolyte, and a cathode aluminum foil. The construction of the anode aluminum foil with an oxide begins with etching the surface of the aluminum foil. Through an electrolysis process, aluminum oxide is deposited on the etched surface. The aluminum oxide is the dielectric. A special paper separator is used to separate the anode from the cathode and is the reservoir for the electrolyte. The electrolyte maintains 100% contact with the aluminum oxide dielectric and the cathode. The life expectancy of an aluminum electrolytic capacitor is determined by the oxide layer. The layer is maintained when a voltage is impressed between the anode and the cathode. With no voltage, the oxide layer gradually migrates in the electrolyte. Over time, the oxide layer gradually erodes and migrates into the electrolyte, thus increasing the leakage current. This leads to heating, which accelerates the process until failure occurs when the oxide breaks down because it is too thin.

Table 2-2 (continued)
Selection of failure mechanisms

Tin whiskers	Tin whiskers are filaments of tin that grow from a tin-plated surface. They grow by addition of material at their base, not at their tip [15]. Whiskers also form in silver, zinc, and gold. The addition of a small percentage of lead reduces the tendency of tin whiskers to grow. With the advent of the RoHS (Restriction of Hazardous Substances) and REACH (Registration, Evaluation, Authorization and Restriction of Chemicals) programs in the European Union, more manufacturers of components are moving away from the use of a small amount of lead and toward the use of pure tin plate. Although the exact mechanism of formation is not known, it is believed to result from residual compressive stresses [15]. Whiskers found on thin tin films (0.5 to 50 µm) are 1 to 5 µm in diameter and can range from 1 to 500 µm in length [15]. Other eruptions, called flowers, extrusions, and volcanoes, can occur on tin surfaces, but they are not as much a concern as whiskers. "Stress may come from the as-plated film with its associated texture … or possibly oxygen diffusion and/or oxide formation on the surface. Corrosion of tin is another possible source for the stress" [15]. The amount of time needed for whisker formations can be minutes or decades and seems to be associated with the length of time for sufficient compressive stress to build up. For more information, see *Current Tin Whisker Theory and Mitigation Practices Guideline* [15], a report published jointly by JEDEC/IPC.

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3
IDENTIFYING FAILURES AND PRECURSORS TO FAILURE

Power plant maintenance programs need to be efficient as well as effective. There is a balance that must be maintained between costs and plant operation. PCBs represent a significant part of a maintenance program. For operating plants, approaches to how they are maintained have already been established. The types of approaches are as varied as there are power plants. How effective and efficient an approach is depends to a large degree on the plant's philosophy and policies.

Some plants are satisfied with the performance of their approaches, whereas others want to improve that performance. As described in Section 1.3, all too often a critical PCB fails in service, causing a plant trip. Generally, there are corrective actions taken when the cause of the board failure can be identified. Power plants are getting older. Components on boards are aging and, as shown in Section 2, some failure rates are increasing with time rather than being strictly random. If the performance of the plant's approach is not satisfactory or if improvement is sought, the following review is recommended.

The review should establish an approach to use in a specific application or system given that the general approach has already been established. Establishing an approach for a specific application is a three-phase process. During the first phase, an evaluation is performed to identify the appropriate approach to use to determine when to replace a PCB. The second phase is the application phase, where techniques applicable to the chosen approach are put into practice. In the third phase, the approach may be adjusted if it does not meet expectations.

3.1 Evaluating PCB Replacement Approach

There are several proven approaches to consider during the evaluation phase. The approach to take depends on the plant policies, procedures, experience, plant design, personnel, and maintenance budget. No one set of standard guidelines can be established that can be used by all plants in every situation. Rather, the following are approaches to consider in deciding the best one to use in a particular situation. These are approaches that have been used in NPPs or in some cases in other industries.

3.1.1 Run-to-Failure

Run-to-failure does not require any monitoring until the PCB fails. This is recommended only for noncritical PCBs or circuits that will not adversely affect the plant's operation. It cannot be recommended if the cost of corrective maintenance and replacement is greater than other approaches. That being said, run-to-failure may be the least expensive approach to managing

PCBs. For operating plants performing this evaluation for a specific PCB or specific system, the review is being done to either improve system performance or reduce maintenance costs and personnel workload. Generally, using the run-to-failure approach will not improve system performance. This approach can reduce maintenance costs and personnel workload. However, before adopting this approach, consider the following:

- The failure does not affect the operation of an important-to-safety system.
- The failure is not a hidden failure that cannot be discovered until the system is called upon to performance a function that is important to plant operation or safety.
- The cost of the corrective action to locate the failure and replace the board is not greater than another approach.
- A replacement board is available in the time that is necessary to bring the system back on line after the board fails. It is important to know the repair time and the consequences of the system being out of service for that time.

3.1.2 Manufacturers' Recommendations

Some manufacturers provide a recommended PCB replacement time or a time when specific components on a board should be replaced, such as electrolytic capacitors. Usually this is conservative, and any failure that occurs before the replacement time recommended would be random and unpredictable. Some manufacturers provide an MTBF or MTTF. If they do, in all likelihood the *parts count* method was used to determine the value. No correlation was found that this method provides a reasonable replacement time. The parts count method is not recommended for a variety of reasons, which are discussed later in this section, but it may be the only method available from the manufacturer. The parts count method is described in MIL-HDBK-217. It is intended by the military that this method be used to provide a figure of merit to compare suppliers' reliability during the bidding process or to assess the change in reliability due to design changes. This is a simple, easy, and, in most cases, cost-effective approach. There are a couple of things to keep in mind, though. The parts count method may be very conservative, and a cost penalty may be incurred related to the cost of a new board. Random failures can still occur before the replacement time is reached.

3.1.3 Plant and Industry Experience

Failure history at the plant, utility, or industry can be useful in determining which PCBs are most susceptible to failures. It is important to maintain information about past failures at the plant. The life expectancy of PCBs is influenced in large measure by the plant environment and maintenance methods. Failures recorded by another plant or the industry may have a different set of environmental conditions and procedures for handling, testing, and storing PCBs. Therefore, the best data are from the plant. Of course, there will be generic issues or failures that are identified in the industry, and these must be addressed.

When reviewing the failure data, look beyond the information for a particular board. Look at the locations of the failures. Are there a lot of failures occurring in a particular area? Check the environment in that area. Temperature increases of 10°C (18°F) can double the failure rate. Are there a lot of failures from one manufacturer? If the failures are broad-based, look at handling, testing, personnel, and storage procedures.

3.1.4 Parts Count Reliability Data

As mentioned in Section 3.1.2, parts count reliability data can be used to establish a replacement time, but there is no correlation between the time calculated and the actual failures in service. The data may be taken from MIL-HDBK-217, the Weibull database, or another available source of reliability data. If taken from MIL-HDBK-217, be aware of the following points about the data listed in the document:

- The data are lumped parameter data rather than distributed parameter data. That is, all of the separate failure mechanisms are lumped together, and the failure rate is calculated for all failures no matter what the mechanism is.
- The failure rate is for random failures only and does not consider wear-out failures.
- Random failures are generally a result of errors or defects in material, manufacturing, operation, design, or maintenance.
- The failure rate given is for the normal region of the life cycle (bathtub) curve.
- The failure rate is taken as a constant value over the entire normal range even though the failure can be random and occur at any time.
- The data for a specific component are generic and cover a range of manufacturers and similar component types.
- Not all of the data are from tests or field data. Some of the values of failure rates have been interpolated to fill in the tables. No indication is given in MIL-HDBK-217 to distinguish which data were interpolated and which came from testing or field data.

3.1.5 Weak-Link Reliability Data

The weak-link approach uses data from MIL-HDBK-217, Weibull, and/or other reliability databases to identify the component that has the highest failure rate on the PCB. The concept is that the component with the highest failure rate has the highest probability of failing first. There is no proof that this is true; in fact, failures can still occur in other components in a random manner before the weak-link component fails. It does provide a method of establishing a replacement time. When using this approach, apply all of the factors that affect the failure rate given in the reliability source being used. It is wise to look at a few different components with high failure rates and apply the factors that affect their failure rates to find the one weak-link component with the highest failure.

Once the failure rate is identified, use Equation 2-1 to find the MTTF. Keep in mind that the probability of a component's survival to the MTTF is only 36%. Depending on the importance of the circuit, the MTTF can be adjusted to a higher probability using Equation 2-3. This can be considered the replacement time. Even with a high probability of survival, there can still be random failures at any time.

3.1.6 Remaining Life Analysis

Remaining life analysis is a calculation of the remaining useful life of a PCB using the conditions the board has been subjected to in the past and projecting the life of the weak-link failure mechanisms, assuming that conditions remain the same as they have been. This approach has been used in a large number of applications in aerospace and the automotive industry. There are a number of service firms that can perform the analysis, each drawing on its experience and database of reliability data for failure mechanisms. Among them is the University of Maryland's Center for Advanced Life Cycle Engineering (CALCE).

In one analysis CALCE performed, NASA wanted to know how many more missions the circuit card in the solid rocket boosters, which control launch, ascent, separation, reentry, and recovery, would be able to complete without failure [16]. To determine the remaining life, an assessment of the conditions to which the board is subjected was first characterized. Using these conditions and analyzing the PCB assembly, the major stressors and weak-link failure mechanisms were established. This was done using CALCE's database of failure mechanisms' reliability data. Notice that the reliability data are for the individual component's failure mechanisms. This differs from MIL-HDBK-217 reliability data, which lump all of the failure mechanisms of a component together. In the NASA application, the major stressor was vibration and shock. The predominant failure mechanism was cracking of the solder connections due to fatigue failure. Using the physics of failure approach, a number of weak-link solder connections were analyzed for their remaining life. NASA thus was able to safely use these boards and replace them before they failed.

The same approach can be applied to any stressor and failure mechanism for a PCB. The analysis should be performed by personnel experienced in using this approach, such as CALCE or another third-party service organization.

3.1.7 Environmental Qualification Data

Systems that are important to safety should have a replacement schedule for any components that have significant aging mechanisms with a life less than the design or qualified life. Almost all PCBs are located in mild environments. If there are components on PCBs, the manufacturer should provide a recommended maintenance or surveillance program. In many cases this is a replacement schedule. The environmental qualification report for the PCBs that have significant age mechanisms should have a replacement schedule.

3.1.8 Maintenance Programs and Guidelines

Maintenance programs can be a source for determining a replacement schedule or a program specific to the PCB being evaluated. If the board falls under the Maintenance Rule, specific actions are required to prevent recurring failures. There may be a plant reliability program in accordance with the Institute of Nuclear Power Operations (INPO) AP-913, from which a replacement schedule may be determined [17]. Guidelines from EPRI may be available for specific PCBs, systems, or types of components. Standard PM templates may be available from industry sources or the manufacturer. These can be valuable resources to use in determining what approach to take.

3.1.9 Trending Calibration Data

Trending calibration as-found or as-left values can be used to calculate drift in the system as a whole. Judgment must be used to determine when the individual PCBs should be examined using other approaches or diagnostic techniques. If the drift from one calibration to another remains relatively constant, there probably are no impending failures. If, however, the drift is increasing between each calibration, a review of the data and possibly the individual boards should be performed. The value of the parameter being calibrated usually has a tolerance beyond which the system is not acceptable. One indication that the individual components of the system should be reviewed is if the drift is so great that the projected drift for the next calibration interval would cause the system to become unacceptable, and the components should be evaluated in greater detail. The drift may be caused by something other than a PCB; it could be the sensor or external power supply.

3.1.10 Functional Testing

Functional testing is an approach that checks the performance of a system on a periodic basis. Generally, this approach consists of mandated tests that are performed to meet technical specification requirements or some other commitment. An unacceptable condition or specification limit is established for the functional test. Going beyond that limit indicates that something in the system has degraded or may have failed. It requires further diagnostic techniques or approaches to identify the degraded or failed component. If this approach is to be used to establish a time when the system should be investigated before an unacceptable condition occurs, a margin can be set on the specification limit. For example, if the function test is to check the response time of a system from sensor input to valve closure, the specification limit may be 30 seconds with a normal system response of 20 seconds. If a margin of 5 seconds is placed on the specification limit, and if the test results are 27 seconds, the system should be investigated further.

3.1.11 Condition Monitoring

One approach that has been proven to identify precursors to failure is condition monitoring. On-line signal monitoring does not have a proven track record, and although research in this area continues, it is not usable at this time. Condition monitoring can be performed by a number of proven diagnostic techniques, which will be discussed in detail later. Many may think of

condition monitoring as an off-line function that requires the circuit to be taken out of service. This is true, but the length of time the circuit is out of service can vary considerably. In some cases, it is necessary to take the circuit procedurally out of service for testing, but in other cases, the testing can be done by computer control, where the circuit is removed from service, tested, and then put back in service. The interval that the circuit is out of service can be long in terms of days, or it can be as short as a few milliseconds. When testing is very short with short intervals between testing, the monitoring can appear to be continuous. An example of this is an automatic radiation monitor check-source in which, under computer control, the following procedure is carried out: the monitor is taken out of service, a source of known value is automatically placed near the radiation detector, the radiation from the source is counted for 1 minute, the counts are checked against a specification limit, and the monitor is placed back in service if it passes the test or taken out of service if an "operation fail" alarm indicates that it has failed.

Before committing to condition monitoring, the question to be answered is this: does it make economic or safety sense to go to the expense of condition monitoring? To answer that question, consider the following:

- Are there other preventive maintenance techniques that can be applied so that condition monitoring is not necessary? It may be more economical to replace the board long before any failure can occur. For example, with aluminum electrolytic capacitors, it may make more economic sense to simply replace the capacitors every 10 years rather than spend the money to monitor their condition on a periodic basis.
- Can the stressor conditions be reduced to increase the longevity of the board? When temperature is the stressor condition, reducing the temperature of the environment the board is in by 10°C can reduce the failure rate by half.
- Is the board a critical component? If it is, there may already be requirements such as calibration trending or operational or functional testing that could be used as condition monitoring.
- If the board is noncritical, is it more economical to run-to-failure and replace the board, or is there a history of failure that is causing expensive maintenance? Is it more economical to condition monitor?

3.2 Identifying Precursors to Failure Using Condition Monitoring

If a precursor to failure can be identified before failure occurs, the board can be removed from service and replaced in a proactive rather than a reactive manner. EPRI has sponsored a number of projects that furthered the goal of identifying precursors to failure. Four of those projects are reviewed in Section 3.7. This section assesses methods that can be used to identify the time when PCBs should be replaced before they fail.

Once it is decided that condition monitoring should be considered, a number of additional questions need to be answered. Figure 3-1 provides a visual representation of the terms used in the following statements (from Society of Automotive Engineers [SAE] JA1012 [18]):

- "There shall exist a clearly defined potential failure [point].
- There shall exist an identifiable potential failure interval.
- The [condition monitoring] task interval shall be less than the shortest likely potential failure interval.
- It shall be physically possible to do the [condition monitoring] task at intervals less than the potential failure interval.
- The shortest time between the discovery of a potential failure [point] and the occurrence of the functional failure shall be long enough for predetermined action to be taken to avoid, eliminate, or minimize the consequences of the failure mode." [18]

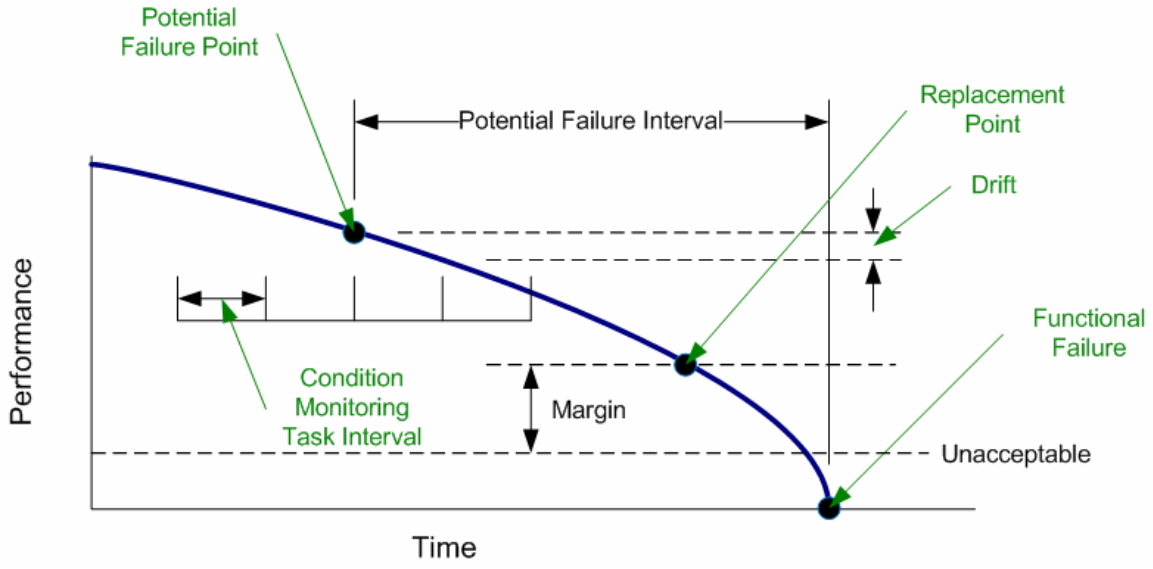


Figure 3-1
Condition monitoring terminology

It is very important that the predominant functional failure and the potential failure point be identified. If they cannot be identified, condition monitoring will not be able to warn of an impending failure. This becomes relatively straightforward with an isolated component, but very difficult at the board and system level.

When monitoring the condition of a component, the performance degradation during the condition monitoring interval is drift. As the component ages, the drift increases exponentially until a point is reached that has been predetermined to be the point at which the board is to be

replaced. The difference in performance from that point to an unacceptable performance is the margin.

Additional guidance is provided from a number of organizations and standards that can be helpful in determining if the SAE JA1012 statements listed earlier are true. Condition monitoring is part of reliability-centered maintenance (RCM), which is in widespread use in the military and industrial communities. EPRI report 1002954, *Guide for Predicting Long-Term Reliability of Nuclear Power Plant Systems, Structures, and Components* [2]; INPO AP-913, *Equipment Reliability Process Description* [17]; SAE JA1012 [18] and JA1011 [19]; and NAVSEA S9081-AB-GIB-010, *Reliability-Centered Maintenance (RCM) Handbook* [20] provide source material for determining which conditions apply in a given situation.

For purposes of this report, it is assumed that the circuit for which condition monitoring is to be performed is known and the condition criteria listed earlier have been met. NAVSEA states:

> Complex items tend to break down through random failure. Complex items contain many simple components, each having its own failure modes. Because there are so many components in a complex item, no single failure mode tends to dominate. Because complex items have a large variety of failure modes, they typically do not exhibit a wear-out age. Their failures do not tend to be a function of age. Failures of complex systems most often occur randomly. Their conditional probability of failure is generally a constant. [20]

In determining the condition monitoring task interval, consider the following:

- Past failures of similar PCBs or components at the plant or in industry. If there is a history of failures in a particular manner in the plant, utility, or industry, the functional failure will be known. Data must also be available to use to determine the potential failure point, condition-monitoring task interval, and potential failure interval. Without this information, conditioning monitoring is “hit or miss.” For this reason, it is important to maintain information about past failures in some retrievable manner.
- Reliability data from a variety of sources. The use of reliability data from sources such as MIL-HDBK-217 and the Weibull databases is not recommended. These databases and their adjustment factors for individual components have been taken from a large population of generically similar components, and all of the failure modes and mechanisms have been lumped together to come up with a failure rate. Combining individual component failure rates by techniques such as the parts count method or even identifying the weak links for a complex board can lead to monitoring the wrong thing, because of the unpredictable nature of random failure.
- The plant’s refueling cycle. This has been the traditional condition-monitoring task interval, and only individual plant experience can determine whether it is an appropriate interval or not. If the specific functional failures of the boards being tested are reduced by monitoring and replacing boards before they fail, it is successful. If, however, there is no reduction in the failures, either the condition being monitored is not correct or the condition-monitoring task interval is too long.

- Calibration data trending. Trending the as-found/as-left data or the drift of the circuit can provide an indication of increasing degradation of components. If the drift is relatively constant or slowly increasing, the circuit is probably aging in a wear-out mode. If the drift is increasing, it may be an indication that something in the circuit is degrading too rapidly and about to fail. The problem is that the component that is degrading too rapidly is not known, and further investigation and diagnostic techniques are required to identify it.
- Commitment to monitor the condition of the printed circuit on a periodic basis. This is similar to the plant's refueling cycle. It is just a preset condition-monitoring test interval other than the refueling cycle, and the same criteria for evaluating its effectiveness apply.
- Fluctuations in the time history of the signal. Unexplained fluctuation in the signal history recorded in a data acquisition system can provide a clue that something in the system is not behaving as it should. It is not known from the fluctuations what the cause is, but it should be investigated to determine whether the fluctuations are due to component degradation.

Identifying precursors to failure at the system and board levels is much more difficult than at the individual component level. Isolated components can be monitored for specific parameters that change over time or that indicate a precursor condition. At the board level, if the component is in series in a circuit, a number of its electrical properties may be measured directly, provided that the impedance of the rest of the circuit is much greater than the impedance of the component being measured. If, however, the component is parallel with other components or to ground, the impedance of the rest of the circuit produces errors in measuring parameters of the component. It becomes even more complicated at the system level. Supporting circuitry, such as power supplies, and additional components in a circuit can include the sensors, displays, computers, programmable logic devices, mechanical control devices, and more.

The ideal diagnostic technique would be one that could identify all precursors to failure while on-line on a continuous basis and sound an alarm to signal that a specific board should be replaced. The proven technology is a long way from being able to do that. Proven technology is able to monitor only by periodic testing, mostly at the board level and not at the system level. Even though a precursor can be measured, a value for the point at which the board must be replaced still must be determined. In the cases when the precursor values are checked periodically, there must be a prediction, with high confidence, of the life remaining in the board to know whether it must be replaced now or can be kept in service for another interval before being tested again.

Even with all of the uncertainty in identifying precursors to failure, experience and the knowledge of actual plant failures can be helpful in trying to determine what to condition monitor. Table 3-1 lists components and their known failure mechanisms. It identifies those that may be monitored and the techniques that may be used to monitor them at the component level. When looking at the board level, the components with monitorable failure mechanisms can be identified, and the measurable characteristics can be projected to the board level.

For consistency, the following are definitions of the terms used in Table 3-1:

- Failure mechanism: the chemical, physical, or material process that leads to a component failure
- Aging mechanism: the specific process that changes the characteristics of a component with time or use
- Precursor to failure: the condition that indicates that a component is going to fail
- Measurable characteristic: the component level parameter that can be measured or observed to identify a precursor to failure

Table 3-1
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Batteries (sealed coin)	Seal failure [21]	Seal material embrittlement [21]	Loss of electrolyte [21]	Corrosion on board [1]	Visual inspection
Cable (ribbon)	Dielectric breakdown	Insulation cracking	Embrittlement and cable stiffness	Cracking and stiffness	Visual inspection
Capacitors (aluminum electrolytic)	Seal failure [22]	Pressure buildup due to chemical reaction between aluminum dioxide and water in the electrolyte [22]	Electrolyte leakage Drift of capacitance and ESR beyond specification tolerance [22]	Electrolyte outside package or on PCB Capacitance ESR	Visual inspection Specific parameter monitoring
	Oxide deterioration	Oxide migration into electrolyte	Increase in leakage current	Leakage current	Leakage current testing
	Dielectric breakdown [23]	Oxide migration into electrolyte	Increase in leakage current	Leakage current	Leakage current testing
	Internal connection failure [23]	Fatigue due to thermomechanical stresses	Crack in connection	None	None
Capacitors (electrolytic tantalum) (also see aluminum electrolytic capacitors)	Seal failure [12]	Lead bending stresses seal area thermomechanical stresses due to charge/discharge [12]	Electrolyte leakage Drift of capacitance and ESR beyond specification tolerance	Electrolyte outside package or on PCB Capacitance ESR	Visual inspection Specific parameter monitoring

Table 3-1 (continued)
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Capacitors (solid tantalum)	Cracks in oxide due to crystallization	Impurities cause localized heating, causing crystallization	Leakage current increase	Leakage current	Leakage current testing
Capacitors (ceramic)	Ceramic cracking	Thermomechanical shock [12]	Decrease in insulation resistance [12], which increases leakage current	Leakage current	Leakage current testing
	Delamination	Degassing organic binding agents by heat during manufacture [12]	Decrease in insulation resistance [12], which increases leakage current	Leakage current	Leakage current testing
	Dendrite and conductive anode filament growth resulting in dielectric breakdown	Ionic migration caused by electric potential in the presence of moisture and manufacturing defects (impurities and bubbles)	Decrease in insulation resistance resulting in an increase in leakage current	Leakage current	Leakage current testing

Table 3-1 (continued)
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Capacitors (plastic, mica)	Dendrite and conductive anode filament growth resulting in dielectric breakdown	Ionic migration caused by electric potential in the presence of moisture and manufacturing defects (impurities and bubbles)	Decrease in insulation resistance resulting in an increase in leakage current	Leakage current	Leakage current testing
	Internal connection failure in metal case capacitors [12]	Fatigue due to thermomechanical cycling	Cracks in connection	None (not visible)	None
	Corrosion of internal metal parts in plastic case capacitors [12]	Chemical reaction due to humidity in the presence of an applied voltage	Reduction of metal volume and presence of corrosion by-products	Increase in resistance resulting in increase in heating	Thermography
Connectors (edge, relay, and IC sockets, multipin on PCB)	Eroded conductive surface	Wear due to mating and unmating cycles [1]	Increased resistance [22] Increased heat due to higher resistance	Contact resistance Temperature	Specific parameter monitoring Thermography
	Contact contamination [22]	Non-age-related error-induced deposits from handling	Increased resistance [22] Discoloration	Contact resistance Discoloration	Specific parameter monitoring Visual inspection
	Dendrite and conductive anode filament growth resulting in dielectric breakdown	Ionic migration caused by electric potential between pins in the presence of moisture and insulation surface contaminants	Decrease in insulation resistance resulting in an increase in leakage current	Leakage current	Leakage current testing

Table 3-1 (continued)
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Connectors (edge, relay, and IC sockets, multipin on PCB) continued	Part loosening leading to an open circuit or grounding intermittent (noise)	Thermomechanical cycling	Loose parts	Loose parts	Visual inspection
	Corrosion	Corrosion buildup due to cleaning solution or environment [24]	Corrosive material on contacts	Corrosive material on contacts	Visual inspection [24]
	Plating peeling on contacts	Contaminants during plating or overheating	Peeling or flaking of nickel plate over copper [24]	Peeling or flaking of nickel plate [24]	Visual inspection [24]
	Bad crimp or solder connection	Thermomechanical cycling	Gradual loosening of the connection	Intermittent	Visual inspection [24]
	Loss of insertion force	Wear or loss of spring load due to wear	Connectors mate without much force	Connectors mate without much force	Visual inspection [24]
	Pitting of contacts	Arcing of contact	Unplugging while energized	None	Visual inspection
	Fretting corrosion	Oxide buildup at connection due to small movements of contacts (vibration) [24]	Oxide buildup Increased resistance	Intermittent resistance	Visual inspection Specific parameter measurement
	Galvanic corrosion	Galvanic potential between dissimilar metals	Corrosion buildup (purple plague) Increasing resistance	Corrosion present Resistance	Visual inspection Specific parameter measurement

Table 3-1 (continued)
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Connectors (edge, relay, and IC sockets, multipin on PCB) continued	Loss of contact float	Loss of the ability to center pin in the spring contact causing increasing resistance and overheating	Increasing resistance Overheating	Resistance Temperature	Specific parameter measurement Thermography
Crystals (Quartz)	Crystal cracking [1]	Non-age-related mechanical stress due to handling [1]	Increased leakage current	Leakage current	Leakage current
	Seal failure [1]	Non-age-related mechanical stress due to handling [1]	Increased leakage current	Leakage current	Leakage current
Diodes (light-emitting diodes [LEDs])	Dark spot formation [25]	Crystallization due to joule heating in high electric field	Decrease in light emission	Light emission	Visual inspection
	Case discoloration	Plastic case becomes opaque with time	Decrease in light emission	Light emission	Visual inspection
Diodes (power)	Cracks in solder connections	Embrittlement due to thermal cycling	Overheating	Temperature	Thermography
	Cracks in silicon die	Microcracking due to stresses during thermal cycling	Increase in leakage current	Leakage current	Leakage current testing
	Contamination of silicon	Manufacturing defect: electrical charges trapped in junction interfaces	Increase in leakage current	Leakage current	Leakage current testing

Table 3-1 (continued)
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Diodes (power) continued	Corrosion of internal metallic contacts	Corrosion buildup and eroding contacts	Thyristors—increase gate threshold current and voltage Transistors—input impedance change	Gate threshold current or voltage Input impedance	Specific parameter measurement Specific parameter measurement
Liquid crystal displays (LCDs)	Pixel failure	Dot electrode failures due to diffusion between n-p material	None	Dark pixel	Visual inspection
Electron tubes	Anode gold evaporation	Anode heating caused by electron kinetic energy	Reduced anode current and power output	Anode current	Specific parameter measurement
EPROM (see also silicon-based active components)	Loss of memory bit	Loss of electric charge due to degradation of oxide grid [12]	None	Lose of memory bit	Computer parameter monitoring (checksum)
Inductors	Ferrite core fracture	Non-age-related vibration or shock causes fracture the ferrite core	None	Inductance change	Specific parameter measurement
Opto-couplers (see also silicon based active components) [12]	Degraded photon output	Photon gradually decreases due to increase of energy traps	Decrease in LED diffusion current and an increase in LED recombination current [12]	LED current	Specific parameter measurement

Table 3-1 (continued)
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Potentiometers	Oxide on coil or wiper	Oxidation of copper	Intermittent resistance change [1]	Resistance	Specific parameter measurement
	Wear of coil or wiper [1]	Wear	Intermittent opens [1]	Resistance	Specific parameter measurement
Printed circuits (boards)	Dendrite and conductive anode filament growth resulting in dielectric breakdown	Ionic migration caused by electric potential between pins in the presence of moisture and insulation surface contaminants	Decrease in insulation resistance resulting in an increase in leakage current	Leakage current	Leakage current testing
	Carbonization of surface leading to dielectric breakdown	Overheated components cause insulation to char and carbonize	Char and carbonized area on board surface Overheated components	Blackened area Temperature	Visual inspection Thermography
	Contamination or corrosion	Buildup of contamination or corrosion on the surface of the board	Increase leakage current	Leakage current	Leakage current
	Delamination of conductive paths	Thermal cycling and poor adhesion can cause traces and edge connectors to lift and crack	Lifting traces	Lifting traces	Visual inspection
	Cracks in traces	Stress and thermal cycling cause traces and pads to crack	Cracking in traces	Cracking	Visual inspection

Table 3-1 (continued)
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Printed circuits (flexible)	Cracks in traces	Stress of bent traces and thermal cycling causes cracking of traces	Cracking in traces	Cracking	Visual inspection
	Electrochemical migration [13]	Electrochemical ionization in the presence of applied voltage causes the trace metal to form conductive filament from the anode to the cathode	Increase in leakage current	Leakage current	Leakage current testing
	Delamination of conductive paths	Thermal cycling and poor adhesion causes traces to lift and crack	Cracks in traces	Cracking	Visual inspection
Relays (electromechanical)	Coil burnout	Coil insulation embrittlement	Charring of coil covering Overheating	Coil covering discoloration (where visible) Temperature	Visual inspection Thermography
	Contact wear out	Thermomechanical operating cycles	Increased contact resistance	Resistance	Specific parameter measurement
	Contact contamination	Contact surface area reduction	Increase resistance [22]	Resistance	Specific parameter measurement
Relays (solid-state) (see also silicon-based active components)	Excess leakage current [1]	Increasing leakage current [1]	Increase leakage current	Leakage current	Leakage current testing

Table 3-1 (continued)
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Resistors	Overheating [1]	Carbonization Increased temperature	Increasing discoloration Increased temperature	Discoloration Temperature	Visual inspection Thermography
	Corrosion [12]	Moisture intrusion	Increasing resistance Noise	Resistance Noise	Specific parameter measurement
Resistors (Metal film)	Contact separation from metal film	Metal film resistors caused by thermal cycling	None found	Open circuit	Specific parameter measurement
Resistors (carbon)	Humidity absorption [1]	Discoloration [1]	Lower resistance below specification	Resistance	Specific parameter measurement
Silicon-based active components (ICs, transistors, operation amplifiers, regulators, logic circuits, TTL digital, linear, CMOS, NMOS, opto-isolators, RAM, ROM, EPROM, signal diodes) [12]	Silicon defect	Temperature creates unexpected generation-recombination centers modifying the life of the carriers [12]	Increasing leakage current Increasing resistance Gain drift	Leakage current Resistance Gain	Leakage current testing Specific parameter measurement Specific parameter measurement
	Grid oxide defect	Breakdown of grid oxide due to temperature and electric field over time	Injection current increase	Injection current	Specific parameter measurement
	Dendrite and conductive anode filament growth resulting in dielectric breakdown	Ionic migration caused by electric potential between pins	Decrease in insulation resistance resulting in an increase in leakage current	Leakage current	Leakage current testing

Table 3-1 (continued)
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Silicon-based active components (ICs, transistors, operation amplifiers, regulators, logic circuits, TTL digital, linear, CMOS, NMOS, opto-isolators, RAM, ROM, EPROM, signal diodes) [12] continued	Ionic contamination	Surface charge ionic migration due to temperature, electric field, and current density over time [12]	Increasing leakage current Gain drift	Leakage current Gain	Leakage current testing Specific parameter measurement
	Electromigration	Electron momentum in conductors in high current densities knock ions from their normal position, causing voids.	Increase resistance Overheating	Resistance Temperature	Specific parameter measurement Thermography
	Hot carriers	Holes or electrons migrate from their normal position, leaving voids leading to instability	Increasing leakage current Increase threshold voltage	Leakage current Threshold voltage	Leakage current testing Specific parameter monitoring
	Internal connection failure	Fatigue due to thermomechanical cycling	Cracks in connection	None (not visible)	None
Solder	Tin whiskers	Growth of tin whiskers	Visible tin whiskers under magnification	Observable tin whiskers under magnification	Visual Inspection
	Fatigue cracking	Thermal cycling causes microcracks to form at high stress areas	Cracks in connection	Visible cracks	Visual inspection
	Corrosion	Corrosion buildup due to flux or environment	Corrosive material on solder connections	Corrosive material on solder connections	Visual inspection

Table 3-1 (continued)
Diagnostic techniques to measure precursors to failure

Component	Failure Mechanism	Aging Mechanism	Precursor to Failure	Measurable Characteristic	Diagnostic Techniques
Solder continued	High-resistance connection	Growth of intermetallic layer between copper and tin	Increase of connection resistance	Resistance	Specific parameter measurement
Switches and keyboards	Contact oxide formation	Oxidation of copper	Intermittent resistance change	Resistance	Specific parameter measurement
	Contact wear	Wear	Intermittent opens	Resistance	Specific parameter measurement
Terminal blocks	Screw loosening	Thermal cycling and vibration causes parts to loosen	Intermittent opens	Resistance	Specific parameter measurement
	Bad wire crimp	Crimp loosens and wire pulls out over time	Intermittent opens	Resistance	Specific parameter measurement
Transformers	Winding open circuit	Thermal stress in winding due to temperature cycling	None given in reports	None—sudden failure open circuit	None
Transistors (power) (see also silicon-based active components)	Crystal microcracking	Microcracking growth due to thermal cycling [1]	None given in reports; eventually microcracking leads to PN junction failure	None given in reports	None

Notes: TTL = transistor–transistor logic; CMOS = complementary metal oxide semiconductor; NMOS = N-channel metal oxide semiconductor; RAM = random access memory; ROM = read-only memory; EPROM = erasable programmable read-only memory; ESR = equivalent series resistance.

3.3 Identifying Intermittent Failures

Identifying intermittent failures can be a very frustrating task, particularly when the intermittent failures only occur occasionally. A number of the diagnostic techniques described in Sections 5 and 8 can be used to help identify the cause of intermittent failures. Usually an intermittent failure will appear in an operating system and manifest itself as an alarm or spike in the output process or instrument loop that will cause an unwanted action to take place. There are two general types of intermittent causes: hardware-related and software-related. There are also repeatable and random intermittent failures. Most PCB assemblies and all software intermittent failures are repeatable. Random intermittent failures are almost entirely the result of components about to fail internally [26].

Repeatable intermittent failures have a trigger. They may not appear to be repeatable only because the trigger does not occur regularly. True random component intermittent failures will eventually become hard failures, which can be found using the techniques described in the next section. However, until the component fails, it may appear the same as a repeatable intermittent failure with a trigger that does not occur regularly.

Everyone has a process for identifying the cause of intermittent failures. Experience and skill are the best teachers. When troubleshooting an intermittent failure, it is best to use a very experienced and skillful instrumentation and control (I&C) technician who knows the system for the task. The following are suggestions for those who may need extra help:

1. Gather as much preliminary information as you can when the intermittent failure occurs.
2. If you do not know the system well, learn as much as you can from loops, schematics, manufacturers' manuals, people who do know the system well, peer groups from other plants, and so forth.
3. If there is not much information or data about the intermittent event(s), consider connecting a time history recorder to the circuit output. Be sure that the response of the recorder is fast enough to record the intermittent event when it happens. Look for patterns, specific times of day, times when specific equipment is cycled on or off, and times when specific procedures or operations are being performed. Look for anything that might be an external trigger.
4. Start with a plan. It does not have to be written, but know ahead of time how to proceed. Be pragmatic and very systematic. This is a process of elimination until the cause and the failure are found.
5. Start a checklist of potential causes. This should be written and added to as new causes are thought of. It is recommended that an I&C binder be kept with the notes from each intermittent and hard failure troubleshooting session. The notes can be a source for potential causes for similar intermittent failures. Some causes to consider are connections (solder, traces between solder pads, sockets of ICs and relays, cabling, edge boards, and plug connectors), EMI, power supplies, and more.
6. For each cause, determine how to determine whether the item is the actual cause of the intermittent failure. Because most intermittent failures are repeatable, apply various triggers to determine which triggers could be associated with the cause. For example, if the intermittent failure is caused by a crack in a solder connection, a trigger that could be

associated with that may be heat or cold or physical movement. Determine the order to perform the tests, taking the most frequent cause that the plant has experienced, starting with the easiest to perform first.

7. Perform the tests is a logical manner, being careful to note anything that is not what would normally be expected. Something seen during these tests may lead to other tests that reveal the problem. Add to the checklist things that come to mind as the tests are being performed.
8. Continue this process until the source of the intermittent failure is found or a dead end is reached. If a board is suspect and one is in stock, replace the board. If the problem still cannot be found, consider replacing boards with available good boards, and look at the boards replaced on a bench to find the intermittent failure rather than trying to find it in the system.
9. If the problem still exists at the system level, it may be time to call in service technicians from the manufacturer or an outside third-party service company.

The boards removed from the system for further examination should be checked using the following diagnostic techniques, described in Sections 5 and 8:

- **Manual visual inspection** (Section 5). Inspect the board, using magnification and looking for the visual signs of the cause of the intermittent failure. In particular, look for cracks in solder connections and traces on the board. Use the list of things to inspect in Section 5.
- **Thermography** (Section 5). Power up the board, and after a warm-up period, take a thermal image. Look for hot or cold spots at solder connections, traces, and components that are not normal. If available, compare the image with a previously taken image of the board. Place a small amount of pressure on the board in different areas to cause it to flex. Doing so may open a crack that is causing the intermittent failure. This could show up as a change in temperature at the crack location.
- **Specific parameter monitoring** (Section 8). With board power on, monitor the board using a time history recorder to determine whether the board is the component in the system that is causing the intermittent failure. To induce the intermittent failure to occur, try raising the temperature of the components using a heat gun or try reducing the temperature using cool air. If the intermittent failure is present from the time history and it cannot be found using the methods just described, perform a burn-in. If the intermittent failure is the early sign of a component failure, a burn-in can cause the component to fail and other techniques can be used to identify the failed component.

3.4 Identifying Failures

Failures, unlike precursors to failure, have a specific known condition that can be measured. The failed component has a short circuit, an open circuit, a degraded condition beyond specification tolerance, or a loss of function. Most of the diagnostic techniques described in Sections 5 through 8 can be used at either the system level or the board level to identify the failure. Keep in mind that there can be more than one failure in a cascade effect or that the failure may be a hidden failure occurring only when a demand is placed on a portion of the circuit.

Identifying failures uses the same approach as was used to identify the cause of an intermittent failure. The difference is that the failure is constant, making the search easier. Failures normally occur in the system while operating or when the system is functionally tested. The approach is to determine first whether the failure is in a PCB or in another component in the system. As with intermittent failure identification, use experienced personnel to work the problem. Experience is the best teacher, and knowledge gained during previous troubleshooting sessions can be most useful in identifying the present failure.

When troubleshooting a system, it is sufficient to identify only the board on which the failure has occurred. Finding the component(s) that failed should be done at a bench at the board level. Consider the following in the troubleshooting process:

1. Gather information related to the event that identified that a failure in the system occurred.
2. Become familiar with the system from loops, schematics, manufacturers' manuals, people who know the system well, and peers from other plants.
3. From the symptoms of the failure, are there obvious things that can be checked easily and quickly that might be the cause? Check fuses or breakers that may have tripped. Check the output from the power supplies to be sure that the system is getting full power.
4. As in the case of identifying intermittent failures, a plan is recommended. Generally, the troubleshooting process is one of elimination. The first step is to divide the system into functional blocks. These can be at the module level (modules containing several PCBs), the board level, or the subsystem level.
5. Assuming that the external devices (such as sensors and electromechanical devices) are all functioning properly, start with a known good input signal to the system. Use signal tracing, described in Section 8, to locate the module or the PCB that has the failed component. If the system is large, such as a nonfunctioning communications loop that has a series of radiation monitors attached, start by disconnecting all of the individual devices and checking the loop without devices attached. Add devices back one at a time until the device that causes the loop to fail is found.
6. When the board or module is found that contains the failed component, replace it and recheck the system's performance. The board should be given a bench test after it is back in operation.
7. At the board level, use signal tracing and signal injection as well as specific parameter measurement to identify the failed component.

The boards removed from the system for further examination should be diagnosed using the following diagnostic techniques, described in Sections 5 through 8:

- **Manual visual inspection** (Section 5). Inspect the board, using magnification and looking for the visual signs of the cause of the failure. In particular, look for cracks in solder connections and traces on the board. Use the list of things to inspect in Section 5.
- **Thermography** (Section 5). Power up the board, and after a warm-up period, take a thermal image. Look for hot or cold spots at solder connections, traces, and components that are not normal. If available, compare the image with a previously taken image of the board.
- **Leakage current testing** (Section 6). If a central utility laboratory is available, check the various components for excessive leakage current.
- **Specific parameter monitoring** (Sections 7 and 8). Check the parameters that can be checked for any that may be out of specification, be shorted, or have an open circuit.
- **Bed-of-nails testing** (Sections 7 and 8). Run a set of functional tests and test as well for shorts, opens, and continuity for the preprogrammed set of parameters.
- **Flying probe testing** (Sections 7 and 8). Run a set of functional tests and test as well for shorts, opens, and continuity for the preprogrammed set of parameters.
- **Signal injection/signal tracing** (Section 8). Use signal injection and signal tracing to locate the point at which the signal is in error. Continue to trace the fault to the component that has failed.
- **IC testing** (Section 8). If the ICs are plugged into sockets, they can be individually functionally tested using this diagnostic technique.

3.5 Diagnostic Techniques Used in Other Industries

Other industries that have to maintain a large number of PCBs are faced with the same problems concerning diagnosis of failure and precursors to failure as the nuclear industry. Due to economy of scale, there are more advances being made in these industries as they relate to both new and existing systems. Development is underway to apply these techniques to legacy systems. The techniques cannot be used directly by the nuclear industry but might be used in the future with additional development.

In the commercial aircraft industry, the supplier of the component or the aircraft manufacturer prepares test procedures that are approved by the FAA for diagnostic testing of avionic systems. In the medical industry, test procedures are prepared by the device manufacturer and approved by the U.S. Food and Drug Administration.

In the past in most industries, the approach has been to run until a faulted or an out-of-specification condition is discovered. As the industries developed and more sophisticated electronics were being used, diagnostic techniques also advanced. One of the first techniques was the use of external diagnostics testers that would automatically test the performance of electronic systems and identify any out-of-specification or faulted conditions. Legacy systems in the aerospace and automotive industries were based on modules supplied by a wide variety of companies that were designed to function together. Each module included built-in testers that

performed fault diagnostics within the module on specific parameters. It became apparent in the late 1980s that as electronics became denser, other techniques would be needed. The idea of the boundary scan was then developed.

Maintenance systems continued to evolve and improve. The older aerospace and automotive industries and the military air, sea, and ground systems are being superseded by newer techniques such as PHM systems.

3.5.1 Boundary Scan Technology

The need to monitor individual test points in the same way as a bed-of-nails tester would—but without removing the board from the system—led to the development of boundary scan technology governed by IEEE Std 1149.1-1990, prepared by the Joint Test Action Group (JTAG). This advancement allowed integrated chip manufacturers to embed, on the chip, a latch at each pin that, under software control, would open the circuit and allow testing of the circuit between ICs as well as between pins on the IC. Figure 3-2 shows a PCB with JTAG-compliant ICs.

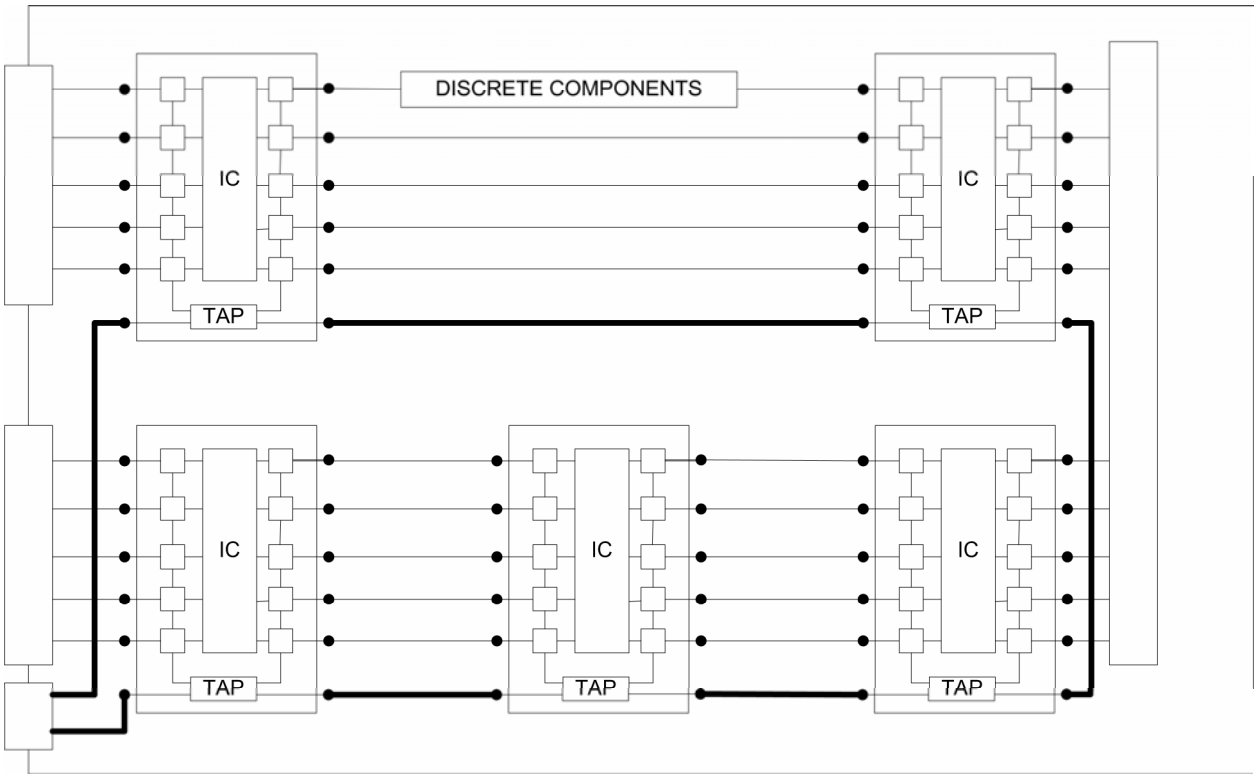


Figure 3-2
PCB with boundary scan ICs

JTAG ICs, mounted on PCBs, have a multiplexer and latch on each pin of the IC. A test action processor (TAP) controller is also built into the IC. Separate access to the TAP is made by a set of pins dedicated to boundary scan testing. In the operating mode, the latches at the pins are closed, and the circuits operate normally. In the test mode, individual pins can be separated

(unlatched) from the IC, and signals injected to test interconnections and functions of the IC as well as trace connections between ICs with JTAG capability. All of the TAPs can be connected in a serial communications loop that can be accessed by a central computer. Discrete components between JTAG ICs or ICs without JTAG capability can also be tested. Thus, under computer control and without the aid of external testing equipment, an entire board or a series of boards may be monitored to whatever degree is desired.

3.5.2 PHM

PHM systems are on board the Joint Strike Fighter F-22 and are finding their way into newer aircraft avionics designs. There are two parts to PHM: system prognostics and system health management. “Prognostics are a predictive diagnostic that includes determining the remaining life or time span for proper operation of a component” [27]. Health management makes “appropriate decisions about maintenance actions based on diagnostics/prognostics information” [27].

Prognostics use algorithms to calculate the remaining life of a PCB, based on stressor service conditions to which the board is subjected. The process begins with an evaluation of the board to determine the weak links and failure mechanisms that could cause the board to fail. In the applications reviewed for this report, the failure of solder connections due to fatigue cracking is the dominant cause of failure in an aerospace vibration environment. The algorithm calculates the life of the board based on the physics of failure of several weak-link solder connections. The vibration of the board could be monitored in service in some manner, such as an accelerometer mounted on the board. Time history response of the board to shock and vibration is fed into the algorithm, and the remaining life is calculated. In the case of the F-22 Joint Strike Fighter, this is done by an on-board system.

Health management includes a computerized maintenance management system that takes diagnostic and prognostic input and establishes maintenance and logistics programs. The system uses the remaining life analysis from the prognostics to determine when a component requires maintenance. This system could be ground-based or on-board.

3.6 Diagnostic Techniques Being Used by the Nuclear Industry

Diagnostic techniques in use in plants indicate the present capabilities of the industry. A survey was sent to a wide variety of plants and facilities that diagnose problems with PCBs. Thirty-four responses were received. The responses were from NPPs in the United States and worldwide, central utility laboratories in the United States, coal plants worldwide, repair facilities, and a manufacturer. The two major categories of interest were the preventive maintenance programs and what type of diagnostic techniques the plants were using.

3.6.1 Preventive Maintenance Programs

The results of the survey for preventive maintenance programs are shown in Table 3-2. The results are divided into four categories for comparison. Even though the central utility laboratories responded to the preventive maintenance program questions, their results are not included because they do not represent the individual plants, and their knowledge may have been secondhand.

Table 3-2
Preventive maintenance approaches of survey respondents

Approach	Nuclear Plants USA		Nuclear Plants Worldwide		Central Utility Laboratories		Coal Plants Worldwide	
	Count	%	Count	%	Count	%	Count	%
Responses	22	65	24	70	3	9	5	15
Replace before failure	8	36	9	38			1	20
Trend calibration data	13	59	13	54			2	40
Manufacturers' recommendations	11	50	13	54			1	20
Past failures	9	40	10	43			4	80
Condition monitoring	5	22	5	21			1	20
Reliability data	4	18	4	17			0	0
No program	1	5	1	4				

As can be seen from the data, there is no consistent approach to preventive maintenance. It is difficult to interpret the raw data to establish trends without further information. Only 36% of those responding indicated that they replaced PCBs before they failed, leaving 64% who run to failure. Yet only one respondent indicated that the plant had no preventive maintenance program. Does that mean that the respondents who did not replace boards before they failed allowed all boards to run to failure or only some boards, because most indicated that they had some basis for replacing boards?

Most plants trend calibration data and replace boards on manufacturers' recommendations. Experience with past failures plays a lesser role, whereas condition monitoring and the use of reliability data play only a small part in determining when boards should be replaced. One plant has established an equipment reliability program in accordance with INPO AP-913 and classifies boards under that program. Others use EPRI guidelines for specific components, but at the same time indicate that they replace when a module fails. One plant uses PM templates as they relate to age and function. Another plant has classified the boards into three levels and assigns a "replace time" to each level. Several plants use environmental qualification information.

The general sense of what the industry is doing is to run to failure except for some boards that are important. Those are replaced on a schedule based on a variety of factors, the dominant one being manufacturers' recommendations.

3.6.2 Diagnostic Techniques

Table 3-3 shows the responses from the industry survey related to the diagnostic techniques that are used. It includes all four categories of facilities: nuclear plants in the United States, nuclear plants worldwide, central utility laboratories, and coal plants worldwide.

Table 3-3
Diagnostic techniques used by survey respondents

Diagnostic Technique	Nuclear Plants USA		Nuclear Plants Worldwide		Central Utility Laboratories		Coal Plants Worldwide	
	Count	%	Count	%	Count	%	Count	%
Responses	22	65	24	70	3	9	5	15
Visual inspection	18	82	20	83	3	100	3	60
Specific parameter monitoring	16	73	17	71	3	100	1	20
Signal injection testing	14	64	15	63	3	100	1	20
Signal tracing	12	55	13	54	3	100	4	80
Dedicated fixtures	8	36	8	33	2	67	0	0
Thermography	8	36	8	33	2	67	0	0
Bed-of-nails testing	5	22	5	21	1	33	1	20
Automatic IC testing	4	18	4	17	0	0	0	0
Flying probe tester	0	0	0	0	1	33	0	0
Leakage current testing	0	0	0	0	2	67	0	0
Automatic optical inspection (AOI)	0	0	0	0	0	0	0	0
X-ray inspection	0	0	0	0	0	0	0	0
Boundary scan testing	0	0	0	0	0	0	0	0
Time-domain reflectrometry	0	0	0	0	0	0	0	0

The predominant diagnostic technique used everywhere is visual inspection. More than 80% of the nuclear plants and 60% of the coal plants use this technique. All of the central utility laboratories use it. The techniques used by most nuclear plants are visual inspection, specific parameter monitoring, signal injection, and signal tracing. All of the central utility laboratories use these techniques. Most coal plants use visual inspection and signal tracing. None of the plants use flying probe testers, and 20% use bed-of-nails testers. Only about a third of the nuclear plants use thermography. Two central utility laboratories use leakage current testing, whereas this is not used in any plants.

3.7 Review of Previous EPRI Reports

Four EPRI projects were completed prior to this project. Each resulted in the increase in knowledge of PCB failures and precursors to failure. When viewed as a group, they address the issue of aging of PCBs and methods that can be used to improve the maintenance of NPPs. As part of this project, the reports resulting from these projects were reviewed for diagnostic techniques that can be used today at NPPs. This section describes the results of that review.

EPRI report 1007916, *Printed Circuit Board Maintenance, Repair, and Testing Guide,* is a practical guide to maintenance and testing of PCBs [1]. Its guidance encompasses troubleshooting techniques and functional testing boards as part of a maintenance program. The report includes test methods that are practical and in use at NPPs.

EPRI report 1003568, *Collected Field Data on Electronic Part Failures and Aging in Nuclear Power Plant I&C Systems,* is phase 1 of a two-phase program to identify test methods to be used to assess aging in components [22]. It consists of a collection of data on selected failures that have occurred at NPPs and identifies their failure mechanisms.

EPRI report 1008166, *Guidelines for the Monitoring of I&C Electronic Components,* is phase 2 of the program [12]. It investigates and demonstrates proof-of-principle test methods for a wide variety of isolated components for use in further research of the effects of aging on these components. For the most part, the test methods demonstrated are for laboratory use and not a plant environment.

EPRI report 1011709, *Evaluating the Effects of Aging on Electronic Instrument and Control Circuit Boards and Components in Nuclear Power Plants,* is a theoretical investigation of generic diagnostic techniques that could be developed and used at the system level to identify the precursors to failure on PCBs [28]. Some techniques require research and development.

The *Assessment of Printed Circuit Board Diagnostic Techniques* project requires that only field-proven techniques be recommended and evaluated in depth in order to identify techniques that can be used at NPPs without further development. To assess the techniques described in the four reports, a set of screening criteria was used. The criteria were the following:

1. The diagnostic technique must be commercially available (equipment or service) or in use at an industrial facility.
1. The diagnostic technique must be able to identify at least one type of failure or precursor to failure for the type of PCBs serviced by NPP I&C personnel.
2. The diagnostic technique must be usable in a plant I&C shop environment.

Criterion 1 screens the techniques presented in these reports to ensure that they are field proven. Proof of principle in a laboratory environment or specially designed one-of-a-kind instruments not available as a service or from an instrument manufacturer were not considered to be field proven.

Criterion 2 screens the techniques to eliminate any that could not identify a failure or precursor to failure on an individual PCB. At the system level, that meant that the technique had to be able to identify that a specific board in the system had failed. At the board level, the technique had to be able to identify a specific component on the board that had failed or had degraded but not failed. Further, the criterion requires that the technique be applied to the type of PCBs serviced by NPP I&C personnel, so techniques used in microwave communications serviced by a communications provider, for example, are not included.

Criterion 3 screens techniques that are generally found in outside service laboratories that perform failure analysis at the component level. For example, techniques such as neutron radiography and energy dispersion spectroscopy would not be included (although a brief description is provided in Appendix C). Techniques such as these are generally not found at NPPs but would be used by outside laboratories during root cause analysis of failed components.

It should be mentioned that these four documents are advancements in the state of the art and provide valuable information as it relates to their objectives. The following reviews include a brief summary of the content of each report and a review of the techniques including the technique's capability to meet the criteria described earlier.

3.7.1 EPRI Report 1007916, Printed Circuit Board Maintenance, Repair, and Testing Guide

This report provides a guide for PCB maintenance, repair, and testing methods. It begins with a description of PCBs, their construction, and their operation. It also includes maintenance practices, repair and refurbishment, and handling and storage of PCBs. Of interest to this project are the sections on component failures, diagnosis and troubleshooting, and testing methods and equipment. The main focus of this report is on failures and troubleshooting failures.

Section 4 of EPRI report 1007916 describes PCB failures. It briefly describes some important concepts related to the causes of failures, the lack of field data for making decisions about component life cycle failures, and the difference between failure modes and failure mechanisms [1]. This section identifies the failure modes for electronic components as open circuit, short circuit, degraded performance, and functional failure. A few selected components were included in Section 4 to identify and describe failure mechanisms for those components. This presents an overview of the whole subject of failures and failure mechanisms with some descriptions of very specific component failure mechanisms. Table 4-2 provides more depth and identifies the failure modes and failure mechanisms for 21 component families that populate PCBs. The information presented in this section is useful in establishing a measurable characteristic that can identify a failure or a precursor of failure. It is not complete, however, and requires additional sources to have a complete picture of the failure mechanisms, failures, and precursors to failure.

Section 6 of EPRI report 1007916 covers diagnostics and troubleshooting [1]. This section provides a comprehensive methodology for troubleshooting boards and introduces the levels of troubleshooting and diagnostics as system level, board level, and component level. The guidance provided for troubleshooting at these levels is brief, with a few tips on specific items.

Section 8 focuses on test equipment and test methods. This section includes a discussion of the test equipment that should be available in any well-equipped I&C shop. The section about dedicated fixtures gives examples of a number of fixtures used to test specific boards. The test methods section for specific devices provides a thorough discussion of the test method that should be used that is unique for that device.

When reviewing the document for diagnostic techniques that would apply to the *Assessment of Diagnostic Techniques* project, a number of techniques can be included:

- Dedicated fixtures for functional testing of specific types of circuit boards. This technique meets all of the criteria. Dedicated fixtures are in use NPPs. Testing their use provides a method for checking signals at different locations on the boards for evidence of failure or degraded condition.
- Visual inspection at system and board levels is a viable technique. It meets all of the criteria. Visual inspections are used in NPP I&C shops. This technique can locate failures (for example, discoloration of the board) and precursors to failure (for example, tin whiskers).
- Signal tracing by dividing the system or circuit in half, finding the functioning half, then drilling down until the failure is found is another technique that meets all of the criteria. Signal tracing is used in many industries, including the nuclear power industry. Using signal tracing, the failed or degraded board (system level) or component on the board (board level) can be located.

- Functional testing is a technique that can locate failures and meets all of the criteria. As described in the first bullet item (regarding dedicated fixtures), functional tests are used in NPPs, they can locate the failed board or components, and they are used to test the functionality of boards after they have been refurbished.
- Specific parameter testing such as the measurement of ripple current on power supplies meets the criteria. Specific parameter testing is used extensively in NPPs to check the condition of power supplies and other devices. The technique can detect degraded conditions, such as high ripple current, which indicates a degraded condition that can overheat electrolytic capacitors, reducing their life expectancy (a precursor to failure).
- Automatic testing equipment (ATE) is a viable diagnostic technique. The discussion in report 1007916 indicates that the equipment is not suitable for NPP and supports that conclusion with a variety of reasons. However, the technique meets all of the screening criteria. There is a variety of ATE available: AOI, automatic X-ray inspection, bed-of-nails testing, and flying probe, to name a few. The equipment is available and used extensively in the manufacture of PCBs. Some equipment, such as bed-of-nails testers, is in use at NPPs. ATE is used to identify unacceptable or failed conditions on PCBs.

3.7.2 EPRI Report 1003568, Collected Field Data on Electronic Part Failures and Aging in Nuclear Power Plant I&C Systems

EPRI report 1003568 is a report of the first phase of a two-phase program to identify methods of monitoring aging in electronic components on PCBs [22]. In phase 1, the project team focused on identifying failures due to aging. They identified families of components that may be affected by aging. They reviewed and documented typical failures from a ranking of components. The team looked at aging management methods in use at NPPs. The report has some usefulness, but it is not a complete investigation of failures and aging management. For example, not all failures and failure mechanisms are described in Section 2, only typical failures and failure mechanisms [22]. Also, the treatment of aging management programs is brief and describes only selected methods of managing the plant's programs.

Section 1 includes two significant tables that can be useful in establishing programs to focus plant resources. Table 1-1 is a ranking of electronic parts found on PCBs and their criticality regarding aging. Six plants were surveyed based on their knowledge of probability of wear out and damage that would be done if the part failed [22]. Thirty components were ranked, with the most critical first. Electrolytic capacitors were unanimously voted the most critical because their standard deviation was zero. As the rankings become less critical, the standard deviations vary considerably. Not all of the respondents agreed, for example, that edge board connectors should be ranked fifth with a mean of 4.5 (out of 6.0) and a standard deviation of 5.5. This leads one to believe that the importance to individual plants of these components can vary considerably. It would have been interesting to see if this ranking would be the same if the number of plants surveyed was larger. Still, the table is useful in establishing a way to focus the investigative effort on those components that are ranked as most important.

Table 1-2 lists the types of errors that can induce failures as PCB components age. This is a useful chart that introduces failure mechanisms that are not a result of traditional age-related failure mechanisms. For example, if the design is not correct, there may be hot spots on the PCB

or component. Increasing the localized temperature causes the component to reach its end of life more quickly and fail. Identifying a design deficiency can be accomplished by using the appropriate diagnostic technique to locate hot spots on a PCB, even if the board is new. This table is important, and the contents must be included when identifying precursors to failure.

Section 2 describes failures that occurred at several NPPs and their associated failure mechanisms. Not all failures that occur at NPPs are included [22]. The sampling of failures is considered typical of the types of failure that occur for these components. Photos of the failure sites and a brief analysis of the failure and failure mechanisms are presented in the order of the ranking in Table 1-1. The discussion identifies the failure mechanism that caused each failure. Table 2-20 lists each component family and identifies the main normal age-related stressor and the main error-induced age-related stressor. This information is useful in identifying what precursors to failure are most important for further evaluation.

Section 3 provides examples of current practices of the six plants that participated, relating to aging management during preventive maintenance, condition monitoring, and repair. It is not considered complete but rather a sampling of those practices. Of particular interest is the assessment of board aging with visual inspection. The inspection gives a rough idea of the aging of the boards and recommends a classification of the boards related to their condition as shown in Table 3-1 [22].

The report recommends that ultraviolet erasable programmable read-only memory (UVEPROM) be reprogrammed every 10 years due to charge leakage through oxides [22]. Even though this is a preventive maintenance and aging management area, it does point out that a failure mechanism is present in the UVEPROM and that the lifetime for reliable operation is 10 years. Erasable programmable read-only memory (EPROM) may be monitored by computer inquiry and a checksum process.

The condition monitoring discussed is an indirect method to determine the environmental conditions of the cabinet in which the board is mounted [22]. The report recommends the use of silver or copper strips that can be placed in the cabinet; the thickness of the oxide layer formed over time can indicate the severity of the environment. Thus, boards in a more severe environment could be inspected more frequently. Table 3-3 classifies four severity levels as defined by ISA 71.04 [29].

This report identifies two diagnostic techniques:

- Visual inspection is a diagnostic technique that meets all of the criteria as described in the previous section.
- Condition monitoring of the type described in Section 3 does not meet the criteria. Monitoring the oxide thickness on copper or silver strips to give an indication of the severity of the environment in which the board is operating does not identify a failure or a precursor to failure. At best, it may indicate that the boards in an area require more inspections than boards in another area.

3.7.3 EPRI 1008166, Guidelines for the Monitoring of I&C Electronic Components

EPRI report 1008166 describes phase 2 of the project reported in EPRI report 1003568 [22, 12]. The report evaluates a number of measurement techniques that can be used to monitor electrical characteristics of components as they age. For the most part, the techniques presented are proof of principle for individual components not attached to PCBs in a laboratory environment. Only in a few cases can the tools be used in an operational condition [12]. Each component identified and ranked is investigated in detail in this phase. A description is included for each component's construction and failure mechanisms. The techniques as well as the results of the experimental measurements are inconclusive. Some techniques are shown to be good indicators of the degradation of components, although others *may* be indicators of aging, requiring further research. The methods and tools presented are designed to be used for continued research into aging of individual components and not designed for use in a plant I&C shop for monitoring the degradation of components on PCBs.

Section 2 looks at each component listed in Table 2-1 of report 1018166 and describes the construction of the component, its failure mechanisms, aging indicators, and tools to measure the aging indicators [12]. It demonstrates proof of principle of tools that can be used for further research. Some accelerated aging tests were performed but only to demonstrate that the tool could actually measure the changes in the indicator as the component was age-conditioned. Results of these tests were inconclusive: of the degree of degradation that occurred before failure occurred was not determined but rather left to future investigation. Most of the tools used in this report were for laboratory use only and required very careful measurements by skilled technicians.

A discussion of each component section in Section 2 follows:

- **Capacitors**. This section investigates capacitors in general, aluminum electrolytic capacitors, tantalum capacitors, ceramic capacitors, paper capacitors, and plastic film capacitors. A general discussion of the functionality of capacitors is presented with their equivalent circuit and the parameters that can demonstrate aging performance of a capacitor. A tool was developed to measure the capacitor's impedance as a function of frequency [12]. There is a claim that the tool could be simplified and used in an industrial application. However, this would require isolation of the capacitor from the parallel impedances of the rest of the board and, therefore, is not practical for plant use. Each specific capacitor type is described in detail with analysis of the failure modes and mechanisms. This provides insight in understanding capacitor failures.

  Tests were performed on aluminum electrolytic capacitors and tantalum capacitors using a tool to measure equivalent series resistance (ESR) and equivalent series capacitance (ESC). Some capacitors were taken from the field, having operated for 10 and 18 years. These were compared to new capacitors. Other new capacitors were age-conditioned at various temperatures for more than 1000 hours. The aged capacitors exhibited drift of both ESR and ESC. Some were considered to have failed because the drift in ESR was so great. However, the work is preliminary and does not provide conclusive data on which to establish guidelines to determine when a capacitor is close to failure. As the authors pointed out, "Additional tests should be done to confirm the fact that this parameter [ESR] is a relevant aging indicator to measure in such aging conditions" [12]. No aging tests were performed on ceramic or paper capacitors.

Plastic capacitors were tested in much the same way as the capacitors described in the previous paragraph. Some were taken from the field after 15 years of operation and compared to new capacitors. Others were accelerated age-conditioned at various temperatures for various times up to 5400 hours. The capacitance drifted due to aging, but the results are inconclusive in that they require additional research to understand their meaning with regard to identifying the end of useful life of these capacitors.

- **Resistors**. Preliminary tests were performed on a precision wire wound resistor aged for several hundred hours at 200°C. Some resistors "burnt" after this age conditioning. There was a significant change in dc resistance between the "burnt" resistors and the aged, but not "burnt," and unaged resistors. It was concluded that dc resistance should be used to monitor aging, but not enough research was done to provide guidance about how to use the dc resistance measurement to determine when end of life is near. The problem is that it is not known when the resistance values changed to an out-of-specification condition. Did it remain in specification until a catastrophic event, such as "burnt," or did it gradually drift to an out-of-specification condition?
- **Active silicon components**. These devices include transistors, operational amplifiers, regulators, and logic circuits that would be found in discrete components as well as ICs. A comprehensive discussion of the failure mechanisms and the underlying physical models that relate to the aging of these components was included.

  For ICs, the diagnostic measurement recommended is the measure of resistance between component pins. This recommendation is not demonstrated by testing or reference to research previously performed. It is an assumption as stated: "It is almost sure however that internal resistance and capacity may drift while aging" [12].

  Discrete diodes and transistors exhibit drift in electrical characteristic as they age [12]. Also, excessive noise is generated as these components age and can be an accurate indicator of aging. However, the report does not recommend performing noise measurements in an industrial environment due to the difficulty in making accurate measurements. It recommends that this be done in the laboratory only [12]. Tests were performed measuring series resistance of diodes at elevated temperatures for various durations as well as for some components taken from the field. The results appear to be inconclusive. The charts that present the results show little change, and no evaluation of them is presented in the report.
- **Operational amplifiers, comparators, and voltage regulators**. A list of measurable parameters is given with no discussion, measurement techniques, or tests performed.
- **EPROM and PROM**. The checksum diagnostic test is the only recommended test for these devices. Also, manufacturers recommend that the devices be reloaded every 10 years. Checksum tests were performed on components that had been in service for 15 to 20 years; half were reloaded, and the other half were not. All were age-conditioned at 150°C and rechecked every 500 hours. All were age-conditioned for 4000 hours (equivalent to 20 years) without failure (except one from those that were initially reloaded). The report states that "EDF NPPs do not have to be reloaded after 20 years and 20 more years of life expectation can be expected" [12]. Forty years without reload when manufacturers recommend

10 years needs to be reconciled. The basis for the manufacturer's recommendation was not included in the report but must be evaluated before a recommendation to industry beyond 10 years should be made.

- **Aged PCBs**. Five PCBs from a Swedish NPP were functionally tested and age-conditioned for 6800 hours at 95°C. The report does not indicate whether the boards were energized or not during the age conditioning. Results of functional tests, inspections, and failure analysis were included in the report. The recommendations and results reported did not provide insight for specific diagnostic techniques or methods for monitoring the performance of aging components.
- **Printed circuits**. This section discusses the various failure mechanisms and degradation on printed circuits. The discussion includes the board and traces, flux waste, dust and corrosion on the board, solder joints, and tin whiskers. The only diagnostic technique recommended is visual inspection with a magnification of at least 5 [12].
- **Batteries**. A great deal of material is presented on aging mechanisms of both primary and secondary batteries used for backup and uninterruptible power supplies on PCBs. Primary batteries are nonrechargeable, whereas secondary batteries can be recharged. The batteries that were investigated are the type that would be soldered to the PCB. Two parameters are identified for monitoring the age condition of a battery: residual storage capacity and internal resistance [12]. The rationale for using these two parameters is based on interviews and literature research.

  There is very little information given regarding the technique to use to measure the internal resistance for primary batteries (residual storage capacity is not relevant). The report states, "Internal resistance of alkaline batteries is usually measured as reduction in closed circuit voltage when the applied load is increased…. The internal resistance is the ratio between the voltage drop … and the discharge current" [12]. An increase in internal resistance is an aging indicator.

  Secondary batteries (NiCd [nickel cadmium]) were tested using two methods: voltage drop and impedance meter. Samples from industry that had been in operation for 20 years were tested. The results show that one battery of the five tested was defective, with a very high internal series resistance. The report recommends that the impedance method, where the impedance spectra are measured as a function of frequency, is the best tool to use. All of the measurements were performed on individual components not connected to a board. Even though the report states "It [impedance measurement] may be used to characterize batteries still on the board," it is not proven.
- **Opto-couplers**. The most relevant indicator of aging for opto-couplers is the current transfer function (CTF), which is the ratio between output current and input current. A reduction in CTF indicates a degradation of the three main parts of the opto-coupler [12]. Very few aged opto-couplers were available from the field because these components are on a replacement cycle and the aged components are not retained. One was reported that showed the shearing of the contact wire. This is an aging failure mechanism that "might not be detected during electrical characterization of the component, until the wire completely breaks" [12].

Extensive accelerated age conditioning was done on a number of components at temperatures up to 150°C for up to 675 hours. A special test setup was developed to monitor the CTF in a plug-in socket. The measurement technique clearly showed the decrease in CTF with time at temperature. Even though this technique could be a promising specific parameter diagnostic technique, it is a proof of principle and not proven in an industrial facility, nor is the test equipment commercially available.

- **LEDs**. Not much was written about these devices. The aging effects in LEDs may be monitored using the CTF as described for opto-couplers, or the emitted power may be measured as an indicator of aging. No other guidance is given, and nothing can be concluded from the information presented.
- **Power components**. The power components identified in the report are those that are devoted to high currents and voltages subjected to high stresses that accelerate physical aging [12]. They include diodes, power transistors, and power thyristors. A discussion of the age-related failure mechanisms was comprehensive. Three aging mechanisms were identified: thermomechanical fatigue, corrosion, and contamination [12]. A literature review and experimental testing determined that the most relevant aging mechanism was an increase of the thermal resistance that manifests itself in an increase in the case temperature [12]. An infrared camera can be used to measure the relative change in the thermal resistance [12]. All other tests would be performed in a laboratory environment on individual components not mounted on a PCB.
- **Electrical contacts—generic**. The devices reported were for low-level voltages and low-level current and included edge board, bolted, crimped, soldered, wrapped, and screw connectors; electromechanical relays; and potentiometers. The discussion of failure mechanisms is excellent. The report identifies the generic failure mechanisms to be corrosion, mechanical wear out, and force contact decrease [12]. It states, "The increase of contact resistance is the most relevant aging indicator for an electrical contact whatever it is" [12]. EDF R&D, Cedex, France (EDF), developed test equipment to measure the contact force using a piezoelectric sensor. They cycled the mating pair of an edge board connector for 2000 cycles and measured the contact force [12]. Not enough testing was performed to be conclusive, and the experiment is considered a proof of principle.

  EDF researched the measurement of the contact/constrictive resistance and determined that the most effective way to perform such measurements was by the nonlinearity measurement, which "basically consists in applying an [asymmetrical] alternating current … through the contact and measuring the residual harmonies of the voltage at the contact terminals" [12]. No measurements were made using this technique; however, it was stated that these measurements were best performed in a laboratory environment, not at a plant site [12].
- **Connectors**. The report describes a number of approaches that could be used to measure the constrictive resistance and connector mating forces. None of the methods described were field-proven techniques, and a number had not been demonstrated with laboratory testing. Visual inspection is the best method that is proven, and the report has a comprehensive table of points to be inspected (Table 2-18) [12].

- **Relays**. This section discusses electromechanical relays in detail. It mentions that there are electronic and other types of relays (opto-coupler, piezoelectric, and thermoelectric) but does not describe them in detail. Tests were performed on electromechanical relays that had been in operation for more than 10 years. Test equipment was arranged to be able to be configured in three configurations: to monitor voltage during closing and opening, to monitor switching duration, and to measure the acoustic signal during switching [12]. The report presents the results and a brief discussion of their significance. The acoustic measurements that monitored the open and closing signal showed the most promise as an aging indicator; however, this is still an experimental method and, judging by the setup and signal manipulation using a fast Fourier transform, a laboratory tool.
- **Potentiometers**. The potentiometer was the last component described in Section 2. This is surprising because it was listed in Table 2-1 as third component of interest by the utilities surveyed. Furthermore, it was given very little treatment and only a brief description with no testing or measurement techniques given.

Section 2 concludes with Table 2-20, which summarizes the components investigated, the measurable parameters, and the tools to make those measurements.

Of interest to the *Assessment of Diagnostic Techniques* project is a statement made in Section 4 for drift measurement [12]. This statement refers to the body of work done in this report. “The measurement of electrical characteristics of components is difficult to perform when the components are still soldered to the board. A test bench dedicated to the measurement of early aging indicators of boards could be designed” [12].

The only two diagnostic techniques that are usable for work at a plant site from this report are visual inspections and infrared examination:

- Visual inspections have been discussed previously.
- Infrared examination or thermography inspection is used in industry, and commercial equipment is available to perform the inspection. It can identify the localized thermal radiation level or hot spots on a board or a component. By comparing images taken of the same board in time intervals, a change in thermal resistance can be detected before the component fails. This technique can be used in a plant environment.

3.7.4 EPRI 1011709, Evaluating the Effects of Aging on Electronic Instrument and Control Circuit Boards and Components in Nuclear Power Plants

Report 1011709 builds on the work of the two previous reports, EPRI reports 1008166 and 1003568 [22, 12, 28]. The report approaches the complex issue of determining the point at which to replace a PCB from a theoretical perspective. It presents a series of six generic methods that incorporate 13 techniques for monitoring the age degradation of PCBs and identifying precursors to failure. The work is comprehensive and includes a decision process recommended for determining the best approach to monitoring the precursors to failure. Some of the techniques are not developed or proven. This presents a problem for the general use of the techniques recommended because the decision process does not distinguish between those that need development and those that have been field proven.

The report relies heavily on the MIL-HDBK-217 parts count method to determine the life of a PCB and alludes to the use of reliability analysis to predict the remaining board life after periodic inspections [8]. The purpose of MIL-HDBK-217 was to provide a consistent method of assessing the design reliability of electronics during the procurement design review phase of military purchases [8]. It establishes a common base for evaluating competitive designs. Its usefulness in predicting component life is doubtful and would require proof to be considered viable.

The report takes the failure analysis work performed in the two aforementioned reports, identifies measurable precursors to failure at the board or system level, and indicates which technique(s) should be used to measure the precursors to failure. The report does not establish a link between measurable precursors to failure and specific failure mechanisms identified in the two previous reports.

The following is a review of the 13 techniques (six methods) against the criteria established to determine each technique's viability for use in plants today:

- **Method 1 periodic inspections—visual inspections technique**. Visual inspections are in use in NPPs and service facilities. Using this diagnostic technique, failures and precursors to failure can be identified. Visual inspections are a proven technique.
- **Method 1 periodic inspections—functional testing technique**. The report identifies functional testing as calibrations and operational checks. Calibrations are performed periodically at NPPs on the electronic system as a whole, from sensor to display. The as-found/as-left information can be trended and the drift determined. The degree of drift can be an indicator of degradation of the system, taken as a whole. This technique does not identify failures because a system cannot be calibrated if it has failed. Furthermore, it does not directly identify a precursor to failure because it is not known what component(s) in the system have degraded. Because it cannot identify the board that is degraded, it is not considered a viable diagnostic technique. It is, however, an indirect diagnostic technique that is discussed in Appendix B.

  Operational checks are performed periodically at the system level to ensure that the system or certain components in the system are functioning properly. It may be a response time check, an alarm set-point check, or the injection of an input signal to the system to determine if the correct values are being displayed. Generally, these are go/no-go tests and do not include quantitative data. They can identify failures but are not as useful in identifying precursors to failure. They can only identify that a system has failed, not the board within the system. Use of operational checks is not considered a viable diagnostic technique. As with calibration, operational checks are an indirect diagnostic technique, as discussed in Appendix B of that report.
- **Method 2 reliability modeling**. The use of a reliability model such as the parts count method is not considered a diagnostic technique for identifying failures or precursors of failures. As mention before, the parts count method was intended primarily as a screening tool for the military to assess the reliability of bidders' designs. The model depends on data gathered on a large population of components, then taking the mean failure rate. The report states, "Determination of an MTBF then relies on generic information that might not apply to the actual operational conditions for the circuit board components in the plant. Thus, a large

uncertainty must be applied to the MTBF and, if a 90% confidence level is used, a board with a nominal MTBF of 15 years might be replaced at 3 or 4 years" [28]. Because it is unable to identify failure or precursors to failure, reliability modeling is not considered a proven diagnostic technique.

- **Method 3 measure of resistance—ground resistance measurement technique**. The theory is that as insulation (between conductive paths and ground) ages, the insulation resistance will decrease and thus can be used to monitor aging. The reality is that the insulation resistance is very high to begin with, and the method commercially available to measure it uses voltages in the order of 700 to 1200 volts dc. This is not usable for assembled PCBs, and therefore, this technique is not considered viable.
- **Method 3 measure of resistance—leakage current testing technique**. As components on PCBs age, their leakage current increases. The leakage current flows in the board's ground circuits to the instrument ground in the cabinet, rack, or module. By measuring the total board or system leakage current to ground and trending the results, age-related degradation can be monitored. Also, by tracing a higher than normal leakage current on the board, a failed component can be identified. Commercial test equipment is available to perform this measurement (Keithley model 6514). Because test equipment is commercially available, the technique can identify failures and precursors to failure, and it is considered a proven diagnostic technique.
- **Method 4 signal comparison measures**. As described in this report, signal comparison measures can be performed on redundant circuits only. These may be in voting logic circuits or in redundant instrument output signals. The comparison of signals may or may not identify a precursor to failure. If the circuits are both aging normally in the same environment, the signal will be degrading at the same rate, and no perceivable difference will be indicated. Thus, redundant boards nearing their end-of-life condition could indicate the same signal level, and the precursor to failure would have been missed. This technique can identify failures in one of the redundant circuits. If one circuit in two out of three or three out of four logic failed, the signal would be out of specification with the other circuits, and thus a failure could be identified. Therefore, this technique is considered a proven diagnostic technique for identifying failures but not precursors to failure, and it is used in plants.
- **Method 5 passive measurement systems—circuit parameter measurement technique**. This technique monitors a circuit or test points on a PCB to identify a change in value indicating a failure or degraded condition. The technique is extensively used at NPPs and testing service companies. It does have the ability of identifying failures and precursors to failure at the system and board level. It is considered a proven diagnostic technique.
- **Method 5 passive measurement systems—environmental parameter measurement technique**. This technique monitors the environment around a PCB for smoke, temperature changes, and other environmental parameters. If a failure occurs, the monitor could signal the presence of smoke or an increase in temperature. Smoke detectors could detect the generation of hydrocarbons at low levels before the complete failure of a component occurs. Temperature detection would be less sensitive to the increase in temperature due to degradation of a component, unless the sensor was at the board near the component about to fail. This does not seem practical due to the density of boards in modules, enclosures, cabinets, and racks. It is considered an indirect diagnostic technique, as discussed in Appendix B.

- **Method 6 active measurement system—current or voltage change technique**. This technique injects a signal in the circuit either at the system or board level. The response of the circuit to that signal is then monitored. Degradation of the response can be trended, or the response can be measured against a specification tolerance, outside of which would indicate a failure. Such diagnostic techniques are used in radiation monitoring systems by using a check source of known value to inject a signal at the sensor end of a monitoring circuit and monitor the output to be within a specified tolerance. Test equipment at the board level could inject a signal using a fixture and measure the response at various test points. Bed-of-nails and dedicated fixtures use this technique to check individual boards by injecting a signal and monitoring test points for responses to be within a specified value. For socket-pluggable ICs, circuit chip testers are available that inject a signal at a pin and measure the response at other pins. Such testers are commercially available and are program-controlled, containing a database of specification requirements for a wide variety of ICs, both digital and analog. Because these techniques are used at NPPs, and they do have the ability to detect failures and precursors to failure, current or voltage change is considered a proven diagnostic technique.
- **Method 6 active measurement system—signature analysis technique**. Signature analysis uses an interrogation pulse injected in a circuit. The return characteristics of the pulse would then be analyzed in the time domain for changes in impedance. Any change in impedance would produce a reflection, the magnitude of which is proportional to difference between the input impedance and the impedance at the point where the impedance changes. A circuit could be characterized initially, and periodically a new measure taken and compared to the initial circuit signature. The exact location of the impedance change can be identified by timing the injection of the signal to the arrival of the response pulse. Changes in impedance could give an indication of aging. Time domain reflectometry (TDR) is in use at NPPs for testing cable run and connections. It could be used for this application. Identifying precursor to failure, however, is unproven and would require development. Identifying failure such as opens and shorts is proven using this diagnostic technique.
- **Method 6 active measurement system—pattern recognition technique**. This technique uses a white noise or pseudorandom input rather than just a pulse. The resulting signature of the reflected signal when displayed in the frequency domain would show a pattern that could be analyzed for condition of the components in the circuit. Although research at universities and at NASA is ongoing (at NASA the technique has been used on the space shuttle to detect faults in gyroscopes and to identify the activation of power consuming devices on the ac power busses), no industrial application could be found or service offered to identify faults on PCBs. The technique is not considered proven.
- **Method 6 active measurement system—frequency analysis technique**. Using a white noise input to a PCB, the output or reflection can be displayed in the frequency domain, and the peaks and valleys of the frequency domain spectrum analyzed for changes that would indicate failed or degraded components. Tektronix does offer equipment for displaying the reflections of input pulse in the frequency domain, known in the industry as s-parameters. Using TDR, s-parameter measurements, circuits may be characterized, and faults such as high data-rate-bit error degradation, jitter, ground bounce, and EMI may be quantified [30]. These are primarily quality assurance measures or troubleshooting techniques. No information could be found that demonstrated that this technique could be used to monitor precursors to failure or failures in the circuits being monitored by NPPs. This is considered an unproven technique.

4
RECOMMENDATIONS

Recommendations for the use of the proven techniques in a plant's maintenance program are provided in this section.

4.1 Recommended Approaches

The following recommendations make up one approach that can be used to determine how to improve the performance of PCBs using this report. Other approaches should be used if these do not fit plant policies or procedures.

1. Review the performance of the plant's PCBs and determine whether the performance is satisfactory or not.
2. Answer these questions to identify systems or PCBs whose performance needs improvement:
   a. Are there boards that have caused plant trips in the past?
   b. Are there systems in which boards are failing too frequently, causing excessive maintenance?
   c. Are there systems that have not failed in the past but whose failure could cause plant trips or extensive maintenance costs, if a board failed?
3. When reviewing past PCB failures, determine whether the board's failure was a result of a component or part of the board failing or whether the cause was external. External causes could have been environmental or induced errors. Section 2 can be helpful in reviewing external causes. The major environmental stressor is temperature. Check the location of the board that failed and determine whether the temperature could have been excessive. The major error-induced cause is handling. Look at the failure and determine whether the failure was caused by mishandling or some other induced error such as ESD. If the failure was externally caused, take steps to correct the cause. Decide whether correcting the cause is sufficient or whether additional measures are needed to improve performance.
4. If the failures are caused by failure of component and parts on a PCB and those failures are not external causes, an evaluation should be performed to arrive at the best approach to use for determining when to replace the board before it fails. Section 3.2 describes a number of methods that can be used to determine when to replace a PCB. Review them and determine which best suits the PCB. If condition monitoring is selected, the following section describes recommended diagnostic techniques that are field proven.

5. Implement the approach selected by documented procedure. Nicholas and Troyer, in their article "Procedure Based Maintenance" concluded, "The more detailed the procedure and the more insistence on compliance with procedures an organization becomes, the more precise and less error prone its maintenance will become. The result will be an increase in reliability" [31]. Increasing the reliability reduces the failure rate; therefore, it is recommended that whatever methods are implemented be done by procedure.
6. If a failure occurs before the board is replaced, review the cause of the failure and adjust the approach or select a different approach to improve performance.
7. Be aware that random failures due to defects can occur at any time without warning. However, the use of one of the methods described here will increase overall performance, reduce the number of failures, and increase plant reliability.

4.2 Recommended Diagnostic Techniques

The diagnostic techniques recommended for use in identifying precursors to failure or failures on PCBs are field-proven techniques. The techniques are in use at NPPs. The techniques recommended are specific. They are not theoretical or generic generalizations. Even though some techniques were found that were in use in other industries, if they did not have a proven field record to identify precursors of failure or failures, they were rejected. One example is AOI. It is in widespread use in PCB manufacturing and can identify cold solder joints, misaligned components, and other manufacturing defects. Two manufacturers of inspection equipment claim that it can be programmed to locate discoloration due to overheating, tin whiskers, as well as other visual indicators of failures and precursors to failure; but it hasn't been done yet. Therefore, it was rejected.

The rest of this section describes the process and criteria for identifying the recommended diagnostic techniques, the organization of the sections that discusses the technique and what is included in those sections, and a listing of the techniques.

4.2.1 Evaluation Process

There are a number of techniques identified in EPRI report 1011709, *Evaluating the Effects of Aging on Electronic Instrument and Control Circuit Boards and Components in Nuclear Power Plants.* These techniques are evaluated, and specific methods for performing the techniques that are field proven are included in this report [28]. To complete the evaluation, a set of criteria is required. The criteria are as follows:

- The diagnostic technique must be commercially available (equipment or service) or in use at an industrial facility.
- The diagnostic technique must be able to identify at least one type of failure or precursor to failure for the type of PCBs serviced by I&C personnel.
- The diagnostic technique must not be used solely for failure analysis.

4.2.2 Organization of Diagnostic Technique Sections

Beginning with Section 5, the diagnostic techniques are assessed in the sequence identified in EPRI report 1011709 [28]. Not every method or technique described in that report is included because many were not field proven.

Each recommended diagnostic technique is described; the methods that can be used are identified when applying the technique; and the ability of the technique to identify failures and precursors to failures is discussed. It should be noted that some diagnostic techniques can be used in more than one way and therefore appear in more than one section.

4.2.3 Recommended Diagnostic Techniques

Table 4-1
Recommended diagnostic techniques

Section 5	Periodic inspections—visual inspection	• Manual visual inspection • Thermography inspection
Section 6	Measure of resistance—leakage current testing	• Leakage current testing
Section 7	Passive measurement system—circuit parameter measurement	• Computer parameter monitoring • Specific parameter monitoring • Bed of nails testing • Flying probe testing
Section 8	Active measurement system—current and voltage change Technique	• Signal injection • Signal tracing • Bed of nails testing • Flying probe testing • Dedicated fixture testing • IC testing • Computer parameter monitoring • Specific parameter monitoring

4.3 Selecting and Using Diagnostic Techniques

After completing the evaluation and concluding that condition monitoring is the approach to use, the question is which diagnostic technique is appropriate. There are three levels that should be considered: system level, board level, and component level. Can any of the three levels be eliminated without further evaluation? For example, the component level is very limited in what can be monitored in a nondestructive manner. ICs in dual in-line package (DIP) sockets could be removed and tested individually, and some parameters may be checked without unsoldering the component from the board, but not many. The following should be considered when evaluating the diagnostic technique to use at each level.

4.3.1 System Level

Aside from calibration trending and functional testing, there are not many options for condition monitoring at the system level. Because boards can be easily damaged by handling, it is recommended that they be touched as little as possible. Many boards are not easily accessible; they may be located in a card cage or rack, or they may be inside an enclosed module. That may mean, at the system level, that condition monitoring can be done only at accessible test points. Consider the following when evaluating which diagnostic techniques to use at the system level:

- **Visual inspection** (Section 5). Visual inspection is the first thing that is done when starting any condition-monitoring process. Whenever a board is in view or partial view, it should be inspected visually for any obvious anomalies.
- **Thermography** (Section 5). Thermography is a diagnostic technique that can identify hot spots on a board or an overheating condition in a cabinet. It is most useful for checking power supplies. An image should be taken that can compare the heat generated by the components on the power supply to the same power supply in a previous inspection.
- **Embedded diagnostics** (Sections 7 and 8). Embedded diagnostics such as computer parameter monitoring are part of the PCB and the system it is in. The manufacturer of the system should be consulted as to the condition monitoring capabilities built into the system.
- **Signal injection and tracing** (Section 8). Signal injection and tracing is a method of checking the condition of boards without detailed probing. Basically, a signal of known value is injected at the input of the system, and values at various test points are measured. There may only be one test point, the output, or there may be several that are accessible. Either the value at the test points has been predetermined, or the values are measured when the system is fully calibrated and the test point values trended at each test interval.

4.3.2 Board Level

Conditioning monitoring at the PCB level offers improved means of evaluating the condition of the board and the best chance of identifying a precursor to failure or a failure. The diagnostic techniques in the following list are for bench testing. The board to be monitored to identify precursors to failure has been removed from service by one of the approaches described in Section 3, has been refurbished and is either being monitored before it is placed in service, or

storage, or is from storage and is being monitored before being placed in service. When evaluating the diagnostic techniques to use at the board level, consider the following:

- **Visual inspection** (Section 5). As can be seen in Table 3-1, a large number of precursors to failure can be identified by visual inspection. The inspection should be performed under magnification by personnel trained to identify the precursors. This should be the first diagnostic performed on any board before other diagnostics are performed.
- **Thermography** (Section 5). A thermal image of an operating PCB can provide a great deal of information about the health of the board, especially when compared to the same board or a good board. Overheating conditions caused by excessive leakage current are detected by comparing an image of the board taken during a previous inspection or a standard good board. The board must be energized to full operating conditions, including output loads.
- **Leakage current testing** (Section 6). Leakage current testing should be done only under laboratory conditions by well-trained technicians. In surveying on industry practices, only utility central laboratories were performing this test. As components and boards age, the leakage currents increase. Comparing leakage current readings from the same board measured during previous testing can give an indication of drift. Table 3-1 lists a number of precursors to failure that can be monitored by leakage current testing. The board must be energized to full operating conditions, including output loads.
- **Specific parameter monitoring** (Sections 7 and 8). Specific parameter monitoring can be performed on some components but not all that are listed in Table 3-1. The problem with this technique is that the balance of the circuit can create errors when measuring a parameter of a component unless the component is isolated. This technique should be used only when the value being measure is not masked by the impedance of the rest of the circuit.

  Using specific parameter monitoring as an active measurement of a voltage or current is an effective way of identifying precursors to failure. Monitoring ripple in a power supply can provide an indication that the capacitors may overheat, thus reducing their life. Checking the current flow or voltage level at the output of a power supply can give an indication of excessive leakage current in a component on the PCB.
- **Embedded diagnostics** (Sections 7 and 8). Embedded diagnostics must be present on the board and must be accessible using bench equipment and software. Some manufacturers provide this information in manuals, but others do not. Check with the manufacturer of the system to see if embedded diagnostics are present on the board, whether they can be accessed, and whether software and/or hardware is available to test the board.
- **Bed-of-nails tester** (Sections 7 and 8). Bed-of-nails testers can be used to test a large number of test points on a PCB. They can be used with the board fully energized or de-energized. Test points should be carefully selected. A balance should be maintained between the cost of the test fixture, the testing time, the software programming (if automatic), and the amount of data obtained. Each different board or change in board configuration requires a different fixture. Readings from previous tests of the same board can be trended for drift.

- **Flying probe tester** (Section 8). Flying probe testers are similar to bed-of-nails testers except that they use one or several movable probe points to accurately access test points on a PCB. The advantage to flying probe is that it does not require a special fixture for every PCB configuration. A disadvantage is the use of fewer probe points. Flying probes can inject a signal at one probe and measure the result at another in the same way that bed-of-nails testers can. The flying probe is less costly than bed of nails to set up but may take longer to run tests and may not be as versatile as bed of nails.
- **Dedicated fixtures** (Section 8) A dedicated fixture is a device that the PCB plugs into or that plugs into interface connections by cables and connector to the PCB. It can be designed and built at the plant site, central utility laboratory, or the manufacturer. It can have built-in input generators and output-testing instruments, computers, and software, or these can be manually added. Dedicated fixtures are used primarily to test the performance of a board as an acceptance test. They may have use in monitoring drift in board outputs.
- **Signal injection and tracing** (Section 8). This technique can be used manually by attaching a signal input to the PCB and measuring the output or by tracing the signal through the board circuitry. It is very useful in troubleshooting and identifying components that have failed or degraded to an out-of-specification condition. The technique can also be used with embedded diagnostics, bed-of-nails testers, flying probe testers, and dedicated fixtures.

4.3.3 Component Level

Component-level diagnostics are limited to those components or functions of components that can be tested in isolation from the rest of the PCB circuitry. It is not recommended that components be desoldered from the board to perform these tests. If the board is manufactured with sockets for individual components, the component may be removed and tested separately. In some cases, measurements across components or between component pins may allow parameter testing. When evaluating the diagnostic techniques to use at the component level, consider the following:

- **IC testers** (Sections 7 and 8). These testers are bench devices that accept the IC pins in a zero-force DIP connector. The testers include specifications for a wide variety of ICs. The device injects the appropriate signal at the input and measures the output. The output is checked against a specification tolerance, and the IC is given a pass/fail test. IC testers are available for both analog and digital ICs. They also can check continuity and measure impedance parameters. They have not been designed to measure precursors to failure but rather to perform acceptance testing.
- **Specific parameter monitoring** (Section 7). At this level, if the component or the measurement can be isolated from the rest of the circuit, the specific impedance values of the component can be measured. By trending the measured parameter's degradation, a precursor to failure may be identified and the component replaced before its failure can affect the performance of the PCB.

4.4 Integrate New Diagnostic Techniques into Maintenance Programs

After the decision has been made to use a technique new to the plant, it should be integrated into the maintenance program. The following recommendations can help establish the technique effectively:

1. Investigate the technique and contact other plants that may be using the technique for their experience and knowledge of its use.
2. Obtain the equipment.
3. Train personnel in using the technique.
4. Prototype the technique on the boards prior to using it on boards from service or stock. Prepare a procedure, a guide, or checklist for using the technique.
5. Use the technique on a small scale first and then expand its use as experience is gained.
6. Assess the effectiveness of the technique after it has been used it for a while. Is it meeting expectations? Should procedures be adjusted to improve performance?

5
PERIODIC INSPECTIONS—VISUAL INSPECTION

Visual inspection is used to examine in detail PCBs for defects that can be seen by the human eye. This section describes this diagnostic technique, where it can be used, what it can find, the methods for using it, equipment needed, personnel requirements, and cost considerations.

5.1 Methods

5.1.1 Manual Visual Inspection

Visual inspection is a staple. It does not require expensive equipment but rather the ability of personnel to identify defects caused by a failure or a precursor of failure on PCBs. Everyone in the plant does visual inspection in one form or another. The inspection may be done with or without magnification. It can be at the system level in the field or at the board level at a bench. It can be routine, as when a cabinet is opened to check dust or contamination on boards, or it can be a detailed board examination under magnification in search of tin whiskers. Whatever level of visual inspection is performed, it is based on what is determined to be necessary for plant safety and operation. Therefore, visual inspection can be categorized as a routine inspection, system-level visual inspection, or board-level visual inspection.

Routine inspection is performed by everyone in the plant being alert to anything that may be out of the ordinary or a deviation from normal. As this pertains to PCBs, it would be done at the system level whenever a PCB is in view. The system may be on- or off-line. Nothing is disturbed or removed during this inspection.

System-level (walkdown) visual inspection is done as a periodic inspection required by plant procedures. This inspection may be part of a preventive maintenance program and include some cleaning and tightening of anything that may be loose. It is more detailed than a routine inspection and focused on specific items to inspect.

Board-level visual inspection is a more detailed inspection of a specific board that has been taken out of the system, taken out of stock, has been refurbished, or has just been received from the manufacturer. It can be done unaided, but magnification is recommended to perform the inspection.

Whenever a PCB is visible, it should be looked at on a routine basis. The obvious things to check for are dust and dirt that may have accumulated on the board. Also check to see if there is any discoloration. Discoloration can be from charring around components that are overheating, corrosion, intermetallic migration, contamination, and a number of other conditions that can be signs of degradation of the board. If in a cabinet with air flow, check to ensure that the air is flowing adequately.

During a walkdown, in addition to the routine items to look for, check the connections for any that appear loose. Perform a more detailed examination of the boards for the items identified for a routine check. Look at cabling for insulation cracking or stiffness. Examine electrolytic capacitors for signs of leaking electrolytes. Look at visible parts of connectors and relay and IC sockets for discoloration. Look at LEDs or displays for decreases in brightness or missing pixels. This level of inspection is not as detailed as that of the board-level inspection, but as much should be done with the unaided eye as possible within reason.

Visually inspecting a PCB at the board level is one of the easiest ways of uncovering precursors to failure. When performing a visual inspection, handle the boards carefully. Use lint-free gloves to avoid contamination by skin oils. Do not stack boards waiting to be inspected on top of each other. Keep boards in static-free poly bags until ready to inspect. Use a ground strap at the bench to eliminate the possibility of ESD, which can cause damage to components that may not be evident for years. When performing the inspection, consider the following:

- When inspecting for workmanship quality, use IPC-A-610D (or latest issue) *Acceptability of Electronic Assemblies* [11]. This document was prepared by the Association of Connecting Electronics Industries. It is a guide that is used by PCB manufacturers to inspect for quality workmanship. It is voluminous, with more than 400 pages of very specific guidelines. Most guidance is done through photographs or illustrations of acceptable conditions versus defective conditions. The document covers anything that can be placed on a board: screw connections, cables, connectors, attaching hardware, as well as good solder connections and component placement. It also covers the handling of boards.

  The level of acceptance is divided into three classes by IPC-A-610D. Boards that are not critical do not have as rigorous acceptance criteria as critical boards. When preparing inspection procedures, it is recommended that a classification be assigned to the board so that it is neither overinspected nor underinspected.

- Magnification should be used for visual inspection. Tables 1-2 and 1-3 of IPC-A-610D cover the strength of magnification to use for different situations. It is recommended that these be followed unless the board manufacturer has specified a magnification to use. The magnification ranges from 1.5X to 20X, depending on size of the lands (component solder pads).

The boards should be inspected for the following precursors to failure:

- Batteries (sealed coin) may be included in some ICs, particularly flash memory. Check around ICs that may contain batteries for signs of electrolyte leakage.
- Cables, ribbon cable in particular, should be checked for signs of embrittlement and cracking.
- Electrolytic capacitors should be checked for electrolyte leakage and cracking around the seal area.
- The connector contact area should be checked for contamination, corrosion, plate peeling, pitting, fretting, and wear.
- LEDs should be checked for case discoloration or the plastic becoming opaque.
- The board surface should be checked for discoloration and charring.
- The traces should be checked for delamination and cracking.
- Relay coils should be checked for charring on the outer package of the coil.
- Resistors should be checked for charring or discoloration.
- Solder connections should be checked for cracking and corrosion, and lead-free solder for tin whiskers.
- All pure tin surfaces should be checked for tin whiskers.

5.1.2 Thermography Inspection

Infrared thermography uses a camera sensitive to the infrared spectrum to photograph a powered-up PCB. A thermal image can be obtained showing the areas of hot and cold. This image can be compared to a known good PCB or compared to an image of the same board taken in a previous test. Both failures and degradation can be identified.

As components age, leakage currents increase within components on the PCB between conductive paths and from a conductive path to ground. In some age-related failure mechanisms, the conductive paths are reduced, thus increasing resistance and causing the location to heat due to current flow. In other cases, short circuits can occur between conductive paths or from a conductive path to ground. These precursors to failure and failures may be located using thermography.

Thermography is a diagnostic technique in use at some NPPs and throughout commercial industries. It uses a digital camera to record an image of the infrared radiation emitted from the surfaces on a PCB. The camera uses an array of microbolometers to obtain the image. A *microbolometer* is a microdevice with a surface material that has a large change in electrical resistance with changes in temperature. Infrared radiation from a location on the object being viewed through the camera lens heats the microbolometer's heat-sensitive surface and changes the electrical resistance of the material held between two electrodes. The electronics of the camera measure the change in resistance at each pixel and produce an image in the visible light range in colors graded to the temperature of the object. The images can be shown on an LCD or saved to a file for later analysis.

Cameras are available in different pixel arrays up to 320 × 240. This provides a detailed image of the PCB. There are cameras that will also display an image in the visual light spectrum of the object that can be superimposed on the infrared image. This allows location of the temperature changes more accurately.

Each material on the surface of a PCB has a different emissivity and therefore gives off a different amount of infrared radiation per surface area than another material at the same temperature. To measure temperatures and the true heating more accurately, images are taken at two different ambient temperatures. Software provided with some cameras analyzes the differences between the two images and provides correction factors for each pixel.

When using thermography, keep the following in mind:

- Use a fixture to maintain a specific distance from the PCB, so that the board is completely in the field of view and the camera is held steady for recording the sharpest image.
- Energize the board and allow it to stabilize. Take care to not introduce errors with air flow across the board. A very small air flow can reduce temperatures. This is particularly important when trying to find intermittent failures.
- Record the image and save it as a digital file for comparison with future images of the same board or same board part number.
- Software is available that can compare two images and produce a difference image, making it easier to identify anomalies. This can save time and provide information on subtle changes that may be missed by a visual comparison.
- Look at components for hotter or cooler spots than expected. Definition of the image has improved in the last few years, and localized heating or cooling on a component can be identified.
- Look at the solder connections for those that may be hotter or cooler than normal. Cracking of solder connections or bad solder connections can be hot because the resistance of the connection has increased, or it may be cool if the connection is completely broken.
- Look at conductive paths and traces on the PCB for the same reasons as the solder connections.
- Look at connectors, relays, and transformers for hot or cool spots.
- Look at the board itself for slight increases in temperature as indications of increased leakage currents.

5.2 Ability to Identify Failures and Precursors to Failure

Visual inspection is one the best diagnostic techniques for identifying precursors to failure and is useful in identifying some failures. Table 3-1 lists the precursors of failure that can be identified by manual visual inspection and thermography. Manual visual inspection is the only way to identify some precursors to failure such as tin whiskers. Overheating of components increases the failure rate, thus leading to premature failures. Discoloration due to overheating can be identified by visual inspection. Short circuit in many cases is accompanied by charring of the

component or the short circuit path. This can be identified by visual inspection. Fatigue cracking at solder connections, in circuit traces, and in cable insulation can be identified using visual inspection. Thermography can identify an overheated condition before failure occurs or a component short or open circuit occurs.

Use of manual visual inspection and thermography together is highly recommended as one of the easiest and most effective diagnostic techniques for identifying precursors to failure and some failures.

6
MEASURE OF RESISTANCE—LEAKAGE CURRENT TESTING

All electronic circuits have a very small amount of leakage from current to ground. As components degrade, the leakage currents increase. As contaminates increase on a board surface, the leakage current also increases. Using low-current-measuring electrometers, the leakage current in ground circuits and from components to ground can be measured. Degradation and failures in the circuit can be identified and traced.

6.1 Description

As components age, generally their leakage current increases and insulation resistance decreases. Leakage current is present in all insulating paths. Usually it is extremely small, and during normal operation, it is not a concern in the operation of the circuit. Measuring it is difficult and requires laboratory conditions. It is not recommended for the plant I&C shop but rather for utility central laboratories. Table 3-1 identifies the components with age-related failure mechanisms that are detectable by an increase in leakage current. There is a total board leakage current that can be a global indicator of aging degradation, but small changes in component leakage currents may be masked by the leakage current from all of the other paths to board ground.

Leakage current is measured with an electrometer and a precision constant voltage source. Electrometers are similar to picoammeters; however, picoammeters in most cases are unable to measure as low a current as electrometers. Electrometers have other built-in measurement functions. Some electrometers have built-in constant voltage sources and are able to read resistance values.

There are two types of electrometer; one uses a shunt resistor, and the other a feedback amplifier that is essentially an op-amp with adjustable gain. Further detail of the operation of electrometers may be found in Keithley Application Note Number 100, *Low Current Measurements* [32]. The range of leakage current is 10^{-8} to 10^{-16} amps. Table 3-1 lists a wide variety of leakage current measurements that are indicators of degradation.

Two approaches can be taken with this technique. One is to monitor the leakage current from several test points that include a number of weak-link components and trend the leakage current readings. The other is to preestablish a level of leakage that has sufficient margin so that a leakage current below that level would be considered a precursor to failure.

6.2 Ability to Identify Failures and Precursors to Failure

Leakage current testing can identify a number of precursors to failure and some failures, but it is not recommended for use in a plant environment. Table 3-1 lists the precursors to failure that can be identified by leakage current testing. The current levels are so small that the procedure for performing the test is very difficult. This should be performed only in a laboratory environment such as a central utility laboratory. It is not a good troubleshooting technique for finding failed components except as a last resort.

7
PASSIVE MEASUREMENT SYSTEM—CIRCUIT PARAMETER MEASUREMENT

7.1 Description

Circuit parameter monitoring is a technique that periodically tests a PCB's component impedances or a specific parameter. At a predetermined measure, the parameter is considered out of specification, and the component or board is replaced. This could be considered condition monitoring. Some computer-based systems monitor parameters on selected PCBs within the system and are able to identify a failed board.

There are basically two passive parameters that can be checked on PCBs: continuity and impedance. They can be measured using manual probing techniques or by using automatic test equipment. They can be used at the system level, board level, or component level. They are useful for troubleshooting failures and have limited usefulness in identifying precursors to failure.

Continuity testing is performed using a low-voltage source and a sensor that completes a circuit when the test probes are placed across a conductive path. If the circuit that the tester is placed across is continuous, the sensor indicates that it is. The continuity test is used for troubleshooting a failure in a system, board, or component.

7.2 Methods

7.2.1 Computer Parameter Monitoring

Computer parameter monitoring is a function that may be a part of a computerized instrument and control system. Generally, the parameter that is monitored is continuity. Impedance can be monitored if the circuitry includes an impedance bridge. This is not common because it adds cost to a system. In a competitive market, only a few may be in use. More common is the monitoring of voltage and current levels by a computer. This is discussed in Section 8.

Continuity can be checked in several ways. If a loop is active, the current or voltage may be checked. The absence of voltage or current indicates a discontinuity, and a failure indication would be initiated by the computer. In the cases when the circuit is not active, the loop may be checked by applying a low voltage to the loop and monitoring it for current. No current would indicate a discontinuity, and the computer would set off an alarm to identify a failed condition.

A computerized instrument and control system functions using an instruction set that continuously loops to monitor sensor inputs and to perform specific functions. Continuity can also be checked during a startup instruction set that would run only one time to bring the system to an operating condition. Checking continuity of a circuit can be part of that instruction set, or it can be a subroutine that is initiated after a specific number of cycles through the instruction set. When a discontinuity is discovered, an alarm subroutine is initiated and the failed circuit identified.

Computer parameter monitoring contains built-in functions that may or may not be described in the user's manual. If the exact functions that are performed are not clearly defined, or if there is uncertainty regarding what functions the computer is performing, contact the manufacturer. Knowing exactly what tests are being performed, and when, can eliminate duplication of tests at the plant.

7.2.2 Specific Parameter Monitoring

Specific parameter monitoring is the measurement of a component's impedance: resistance, capacitance, or inductance. Monitoring specific voltage and current parameters is addressed in Section 8. Measuring specific component impedances to identify precursors to failure manually is difficult for those components that are in parallel with other components. The impedance measure may be the combination of the parallel circuit. Even though some parameters may be measured, unless the component is a weak-link component with a very high probability of failing, the effort to trend measurements is too time-consuming to perform manually.

This method can be used to check continuity, opens, and shorts on a board by using the resistance function of a multimeter. Care should be taken that applied voltage of the multimeter is within the rating of the components on the board.

7.2.3 Bed-of-Nails Testing

A bed-of-nails tester can be used to test for shorts and opens between test points and may be used in certain applications to measure the impedance of a component, provided that the component is not in parallel with other components between the test points. The bed-of-nails tester consists of a series of spring-loaded test pins (pogo pins) mounted on a plastic board in an array that matches the location of points to be tested on a PCB. The pin array board or fixture is brought in contact with the PCB being tested in a holding fixture. In the case of passive measurements, the board is not energized. Under software control, tests are performed between two pins in a predetermined sequence. The results of the test are compared to values stored in the computer, and any anomalies are flagged.

Bed-of-nails testing for passive measurements is generally combined with active measurement, described in Section 8. In this mode the testing is a functional test for components that do not meet specifications or that have failed. One manufacturer (Kimka Inc.) uses a guard circuit that cancels the current flow to parallel circuit components, thus allowing the measurement of passive characteristics of components between two pins. The values of the measurements are stored in a computer file so that previous reading of the same board may be compared.

7.3.4 Flying Probe Testing

The flying probe technique uses a tester that can precisely position one or two probes (spring-loaded test pins or pogo pins) on a PCB. It is an alternative method to the bed-of-nails tester. The probes can be programmed to make measurements at any point on the PCB in any sequence desired. The probes are located on a moveable arm that can position the probe anywhere on the board in an x-y-z position. As with the bed-of-nails tester, continuity, shorts, opens, and some component impedances can be checked. The measurements are compared to normally expected measurements, and thus degraded or failed parts can be identified. The flying probe tester does not require a fixture to hold the test pins as the bed of nails does; therefore, the cost for fixtures is saved, and any changes to a board or test scheme do not require changes to the fixture. The flying probe tester does require additional programming to identify the x-y-z location of each probe for each test. Some flying probe testers have multiple probes for both sides of a board. Some can inject signals at any point as well as make measurements.

7.3.5 Ability to Identify Failures and Precursors to Failure

The passive measurement diagnostic technique does have the ability to identify failures and in some cases precursors to failure. This section describes the ability of each method to accomplish such identifications.

Generally, computer parameter monitoring is a diagnostic method to identify failed components or out-of-specification conditions. In most cases, the monitoring is performed as active measurements, but there may be a few cases that continuity, shorts, opens, and degraded conditions may be checked on a passive basis. Functional failures will not be checked passively. The diagnostics of the computer basis system are built into the system by the manufacturer; therefore, to know the ability of the system for self-checking passive parameters, the manufacturer should be consulted. In most cases, this method does not monitor parameters for degradation to identify precursors to failure. There could be an exception to this, but none is known.

Specific parameter monitoring using manual methods is able to identify failures such as shorts and opens and in some cases degraded components. Even though a number of precursors to failure can be identified (see Table 3-1) using this method, to do so is difficult and time-consuming. Parallel components can introduce errors in impedance readings; therefore, unless the component can be isolated from the rest of the board's circuitry, the measurements will not be meaningful. Furthermore, because the boards can contain a large number of components, it would not be efficient to measure the parameters of all that could be measured. Only the weak-link components should be measured if they can be isolated.

A bed-of-nails tester has the ability to automatically test a board for failures such as continuity, opens and shorts, and degraded components. Except for the Kimka tester, which uses a guard circuit to cancel currents due to parallel components, the bed-of-nails method does not have the ability to identify precursors to failure by measuring component impedances unless the component is isolated from the rest of the board. With the Kimka bed-of-nails tester selected, weak-link components can be monitored for degradation and the measurements recorded on computer file. Components can be compared on a periodic basis for drift of values.

Flying probe testers are similar to bed-of-nails testers for the identification of failures and precursors to failure.

8
ACTIVE MEASUREMENT SYSTEM—CURRENT OR VOLTAGE CHANGE TECHNIQUE

8.1 Introduction

Use of active measurements with the change in voltage or current as an indicator of a failure or a precursor to failure is the primary electrical technique in use today. Testing can be functional or condition monitoring. When performed as a functional test the system, the board or component is energized as it would be in operation, and the various required functions are tested to ensure that they are within specification limits. Functional testing is used primarily to identify failures or out-of-specification conditions in a system, board, or component. Condition monitoring is a periodic test that monitors the changes in voltage or current to identify drift in precursors to failure. It can be done at the system, board, or component level as well. There are limitations to condition monitoring, described in Section 3.

There are a number of proven methods that can be used for both functional testing and condition monitoring. This section describes those methods. They may be used individually or in combination at the system, board, or component level. All of these techniques are used off-line, and even though the system may be energized, the interface with other plant systems is disconnected.

8.2 Methods

8.2.1 Signal Injection

Signal injection can be used for identifying failures of components as well as condition monitoring to locate precursors to failure. This method can be used manually or with specialized test equipment, discussed later in this section. In its simplest form, a signal generator is connected at the sensor input to the system, and the output is observed. Signal injection may be combined with tracing with a known signal injected at the input or some other location in the system, and the circuit's response to that signal injection probed and traced along the circuit to locate the failed or degraded component in the circuit. In analog systems, signal injection can be used to condition monitor the signal at various locations in the circuit. Condition monitoring becomes more difficult for digital circuit due to the pulse nature of the signals. However, signal injection can identify failures in digital circuits.

Signals that are injected can be analog or digital. Signal generators can be used that provide a stable dc input or sinusoidal at various frequencies. Logic pulsers in combination with logic probes may be used on digital portions of the circuit to inject a pulsed digital signal either as a steady high, steady low, single pulse, or pulse train. The probe may be placed downstream of the pulser input to measure the response of the circuit and verify its proper operation.

Before using signal injection, it is essential that the operation of the system be understood and the expected values of the measurement points be known. Use loop diagrams and vendor service manuals to gain an understanding. It may be beneficial prior to troubleshooting a failed or degraded circuit to inject a signal on a known good circuit and measure the points at which measurements are to be made on the failed circuit to establish acceptable values.

Check the power supply outputs, if they are accessible. In some cases the power supplies are contained in an inaccessible module along with the PCB to be tested. This makes it impossible to check the power supplies without taking the module out of the system and opening the case.

At the system level, the objective is to be as nonintrusive as possible to the system in place. There is always a chance of damage whenever modules, boards, or connections are disturbed.

When troubleshooting with signal injection, there are two possible ways of injecting the signal. Both require that the input signal at the system input be disconnected. The first is to inject the signal at the input to the system. The output is measured, and if it does not meet expected results, a measurement is taken approximately halfway between the input and output. If the measured value is good, the problem is in the second half of the circuit, and it is probed in the same manner (halfway between the midpoint and the output). If the value is bad, the problem is between the input and the midpoint, and that section of the circuit is probed further. This process continues until the failure is found.

In the second approach, the signal is injected at the midpoint of the circuit, and the output is measured. If the value is acceptable, the failure is in the first half of the circuit. The signal would be injected midway between the midpoint of the circuit and the input. If the value is not acceptable, the failure is in the second half of the circuit, and the signal would be injected at the midpoint between the midpoint of the circuit and the output. This process is repeated until the failure is located.

In condition monitoring an analog system, a signal of known value is input at the input of the system, and the values at various test points in the system are measured. In the case where this is performed during calibration, the values of as-found and as-left should be recorded. By determining the drift at various test points, the condition of the circuit from the measurement point to the input can be determined.

8.2.2 Signal Tracing

An accurate signal is injected at the input to the system or board. The signal may be the same as the normal signal, or it may be another known signal. Other known signals may be at different voltages or different frequencies. A probe is used to check the signal through the circuit. At the location that the signal does not behave as expected, the board, part, or IC function that has failed or degraded can be identified.

If used for troubleshooting a failed circuit, the same technique as used with signal injection should be used. That is, troubleshooting should begin at approximately the halfway point between the input and the output. This process should continue until the failed board, component, or IC function is located.

If signal tracing is used for condition monitoring, test points should be chosen to monitor the condition of the system, board, or component on the board. Condition monitoring at the system level is not recommended because it would physically disturb the system components. The danger of causing a problem by accidentally shorting a component or causing damage is too great. If, however, it must be done at the system level, isolate the system from any automatic functions that can cause disruption of the plant operation or challenge the safety system. Choose the test points to cause the least disturbance to the system components. Take great care with the signal injected at the input so that the circuit is not damaged by overvoltage conditions.

At the board level, several diagnostic techniques for condition monitoring use equipment described later in this section to automatically check and record the values of voltages at various test points on PCBs. Among these are bed-of-nails testers, flying probe testers, and dedicated test fixtures. As with system-level condition monitoring, the test points must be selected and the values of voltage known.

Signal tracing an analog circuit or the portion of the digital system that is analog (sensor to analog to digital converter) is relatively straightforward. The voltages at the test point can be measured directly. The digital portion of a circuit, however, requires a logic probe that can display or analyze the pulse train as it passes through the circuit. The logic gates of the ICs must be understood to determine whether the circuit is functioning properly. Thus for analog circuits, degradation in voltage can be measured at the test points. Degradation in digital circuits cannot be measured directly; only the functionality may be checked.

8.2.3 Bed-of-Nails Testing

A bed-of-nails tester can be used to test for analog and digital signals between test points. The bed-of-nails tester consists of a series of spring-loaded test pins (pogo pins) mounted on a plastic board in an array that matches the location of points to be tested on a PCB. The pin array board or fixture is brought into contact with the PCB being tested in a holding fixture. In the case of active measurements, the board may or may not be energized. Under software control, tests are performed between two pins in a predetermined sequence. The results of the test are compared to values stored in the computer, and any anomalies are flagged.

One manufacturer (Kimka) uses a guard circuit to cancel out alternate current path, thus isolating the component and enabling the testing of individual components without removal from the board. Typical measurements that Kimka reports can be performed are identifying open diode junctions, leaky diodes, degraded zener voltages, and ICs with low output levels or that do not switch properly with correct input levels. Other tests such as edge-to-edge functional tests are possible with bed-of-nails testers. The measurement values for each test are stored and identified for each PCB tested. Thus measurements of the same board taken over time can be compared, and values that are out of specification can be identified.

8.2.4 Flying Probe Testing

The flying probe technique uses a tester that can precisely position one or two probes (spring-loaded test pins or pogo pins) on a PCB. It is an alternative method to the bed-of-nails tester. The probes can be programmed to make measurements at any point on the PCB in any sequence desired. The probes are located on a moveable arm that can position the probe anywhere on the board in an x-y-z position. As with the bed-of-nails tester, the flying probe tester can perform functional tests of an energized board. Flying probe testers have the capability of signal injection at specific components and measuring the output signal. The measurements are compared to normally expected measurements, and degraded or failed parts can be identified. The flying probe tester does not require a fixture to hold the test pins as the bed of nails does; therefore, the cost for fixtures is saved, and any changes to a board or test scheme do not require changes to the fixture. The flying probe tester does require additional programming to identify the x-y-z location of each probe for each test. Some flying probe testers have multiple probes for both sides of a board.

8.2.5 Dedicated Fixture Testing

A dedicated fixture is a specially designed fixture into which a PCB to be tested may be plugged. The fixture can be supplied by the manufacturer, a third-party supplier, or plant. It is designed to perform a functional test of the PCB and thus the appropriate inputs to fully test the board. Outputs from the board can be measured and the results compared to expected results or specifications. Tests can be manual or automatic. Generally, these are pass/fail tests that can identify failed or out-of-specification conditions. It is left to other diagnostic techniques to identify the component on the board that has failed or is out of specification.

8.2.6 IC Testing

IC testing is a technique that automatically tests the functionality of analog or digital ICs that would mount in sockets on a PCB. The tester can be a handheld or desktop model with a library of specifications for a wide variety of ICs. The IC to be tested must be removed from the PCB and placed in the zero-force connector on the IC tester. There are two types of IC testers: linear for analog devices and digital. A built-in library of IC specifications is used to apply the correct input signal to the appropriate pin and measure the output. The digital IC tester applies input signals to the appropriate pin and monitors the state of the outputs. The output is compared to the specification limits for that function, and the tester indicates a pass or fail condition. The linear IC tester can test operational amplifiers, comparators, switches and multiplexers, regulators,

references, virtual grounds, opto-couplers and isolators, and other analog ICs. The digital IC tester can test transistor–transistor logic (TTL) ICs; complementary metal oxide semiconductor (CMOS) ICs; memory ICs; and interface, peripheral, microprocessor, and large-scale integration (LSI) circuits. The IC is powered by the tester and input signals applied to each pin. The output is measured and compared to the specification values. Functions that do not meet specification requirements are identified.

8.2.7 Computer Parameter Monitoring

Some computer-controlled systems have built-in diagnostics that check functions of the system to determine whether they are operating properly. Examples of these diagnostics can be found in computerized radiation monitoring systems:

- The checksource function is a computer parameter monitored function. Under computer control, a radioactive source of known value is brought into view of the detector and the radiation measured for 1 minute. If the value at the output is within the preset specification tolerance, the test passes. Thus the circuit is checked from the detector to the output to identify an out-of-specification condition.
- In another test, the computer continuously monitors the pulses from the radiation detector. Because the background radiation is always high enough to produce some pulses in the detector in a specific period, the computer monitors the pulses for no pulses within a period. If none are present at the output, the computer sets off an alarm indicating that an operation failure has occurred.

Power supply voltage sources can be monitored as well as other signal parameters. These diagnostics are for failed or out-of-specification conditions. The tests that are performed are those built-in tests that the manufacturer has programmed in the computer. The manufacturer's manuals should be consulted to determine the extent of testing being performed for a particular system.

8.2.8 Specific Parameter Monitoring

Active measurement specific parameter monitoring involves the measurement of specific voltage or currents to identify degradation. In most cases these measurements are used to judge whether a board should be replaced or refurbished. Among the parameters that can be monitored are ripple current or voltage on power supplies. Ripple current in a capacitor will heat the capacitor. If the ripple current is too high, the capacitor temperature will rise and its failure rate will increase.

Power supply current to the PCB can be an indication of degradation of components on the board. As components degrade, their leakage current increases, and thus the board will require more power to operate. If the voltage output of the power supply is held constant, the current draw to the board must increase. This can be an indication of board degradation.

8.3 Ability to Identify Failures and Precursors to Failure

Active measurement for changes in voltage and current is a diagnostic technique that has the ability to identify failures and precursors to failure. Each method that can perform this diagnostic technique is reviewed in this section for its ability to identify failures and precursors to failure.

Signal injection can be performed at the system level and at the board level. At the system level, it is able to identify and locate failures and is one of the primary methods used to do so. It is not as useful at this level in identifying precursors to failure except when used in conjunction with computer parameter monitoring. By injecting a signal at the input of the system and monitoring the output, a degraded condition can be identified. Other methods would be required to identify the board or other component that is the cause of the degradation, however. At the board level, using signal injection at various locations on the board can identify failed components. As with the system level, the injection of an input signal in conjunction with signal tracing can be an effective method for identifying precursor to failure.

Signal tracing, as with signal injection, is performed at the system level as well as the board level. Signal tracing at the system level is an effective method to identify failures and to isolate the board that contains components that have failed. It is less effective at this level for identifying precursors to failure. At the board level, signal tracing in conjunction with signal injection can be an effective method of identifying failed components and also to monitor signal degradation at test points on the board. This can provide a measure of degradation and thus a precursor of failure. To do so, the effect of the degradation on the test points of weak-link components and the point at which the value at the test point that is considered unacceptable would have to be determined.

Bed-of-nails testing is able to identify failures and precursors to failure for many components. Test points are preselected, and they cannot be easily changed. As such, the functionality of the circuit board can be checked through those test points. Failures can be identified as out-of-specification conditions at the test point, and the failed component can be narrowed down to between two test pins. Precursors to failure can be identified by measuring the voltage at the test points and trending readings at the test intervals. Components can be identified for replacement based upon a predetermined replacement point (see Figure 3-1).

Flying probe testing can perform the same functions as the bed-of-nails testing.

Dedicated fixture testing allows the board to be plugged into a tester and a functional test to be performed. It can identify an out-of-specification condition and that a specific function of the board has been found unacceptable; however, other methods are necessary to pinpoint the failed component. Drift of a function can be trended between test intervals and, if the replacement point is known, can be a precursor to failure. This can be done only at the board level; therefore, individual components cannot be trended or a precursor to failure found for them using this method.

IC testers are functional testers that can identify failures but are not able to identify precursors to failure.

Computer parameter monitoring has the ability to identify failures and some precursors to failure. The parameters that are monitored are predetermined by the manufacturer and built into the system software. Specific voltages and in some cases currents are monitored for a degraded or failed condition. Very little is done to identify precursors to failure and computer trending of measurement taken at the appropriate test interval. In some cases the replacement point value has been predetermined by the manufacturer, and when that value is reached, the software flags the condition for operator action. A case in point is the high voltage level for a photomultiplier tube on a radiation detector. The predetermined voltage at which the tube should be replaced is stored in a computer database. The computer control of voltage of the photomultiplier tube in order to establish a specific gain continually adjusts the voltage. As the tube ages, the voltage requirement increases until the predetermined voltage of replacement is reached.

Specific parameter monitoring is an excellent method of identifying failures and some precursors to failure. By measuring voltages or current of components using signal injection, a component that does not measure up to specification tolerances can be identified. By measuring voltages or currents of various circuit elements, precursors of failure can be identified. For example, an increase in ripple in a power supply can be a precursor to capacitor failure because the ripple current in a capacitor will cause the capacitor to heat, therefore reducing its life. Excessive current draw from a power supply can be caused by excessive leakage current on a circuit board or a component that is about to fail.

9
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本報告描述由電力科學研究院 (EPRI) 贊助的研究。

本報告為合編文件，在文獻中引用時應遵循以下方式：

《核電廠維護應用中心：印刷電路板診斷技術評估》。EPRI, Palo Alto, CA： 2009. 1018534.

報告摘要

本專案評估了先前 EPRI 印刷電路板 (PCB)
報告中的技術、理論方法和所提建議，旨在尋求有助於延長 PCB 壽命的技術。

背景

核電廠 (NPP) 使用的印刷電路板 (PCB) 出自不同廠商，結構也各不相同。電廠使用的 PCB 會隨著時間老化，故障次數也隨之增加。所有 NPP 都有管理設備（包括 PCB）性能的政策和維護計劃。PCB
維護計劃的重要性會因其與電廠安全和運轉的關係而異。

儀錶和控制 (I&C) 人員對於 PCB
的結構和使用非常熟悉，但他們有可能不太熟悉電路板層級的故障模式和部件故障。電力科學研究院 (EPRI) 進行了若干項調查，努力開發監測 PCB
性能的方法，以在發生故障前對電路板進行檢測。本專案評估了先前 EPRI
報告中的技術、理論方法和所提建議，著重於以下兩種方法：

- 找出可用於監測個別部件退化的技術
- 找出可開發用於監測電路板和系統性能的理論方法和技術

目的

- 評估用於檢測 PCB 狀況的現有診斷技術
- 確認所建議技術的能力和局限性，及其是否能夠線上或離線確定電路板故障先兆
- 收納現場試驗證明方法、其使用簡易性、設備成本及供應狀況

方法

本專案採用以下方法：

1. 首先，為確定在核電業以及其他產業中使用的經過證明的技術和診斷技術，對先前的 EPRI 調查進行評估。
2. 調查 PCB 部件故障的性質。
3. 針對技術選擇，制定評估標準。
4. 對商業測試設備和技術進行審核。
5. 對本產業進行調查，確定預防性維護計劃應採用的方法和診斷技術。
6. 對其他產業的診斷技術進行調查，找出管理 PCB 壽命週期的最新方法。
7. 審核各項技術確認故障和故障先兆的能力。

結果

本專案所得結果如下：

- PCB 故障是隨機發生的。有些隨機故障與老化有關，因此可以監測出 PCB 退化情況，而有些故障不可預測，隨時都可能發生。隨著製造流程品質的改善，與老化有關的不可預測故障次數已有所減少。
- 要監測 PCB 所有故障模式是不可能的。軍事、航空和汽車業所採用的方法是確認薄弱環節部件，並以此為基礎建立維護計劃。
- 找出了新方法來判斷更換電路板的時間，即剩餘壽命分析，該方法廣泛應用於軍事、航空和汽車業。
- 軍事、航空和汽車行業透過預測學和健康狀況管理計劃來解決此問題。此方法廣泛應用於 F-22，並且越來越普遍用於機載航空電子設備和汽車電子系統方面。最終目標是讓健康狀況自動管理電腦監測診斷（與技術規範不符的條件）和環境條件。這樣會減少外部測試的需求。
- 建議採用一系列經過證明的診斷技術。目前美國核電廠只使用了其中部分技術，因此可以用來加強電廠 PCB 預防性維護計劃。

EPRI 遠景

本專案著手完成先前 EPRI 報告中開始的工作，旨在開發出一套可以方便用來監測 PCB 狀況的診斷技術。

儘管評估結果並未得出 PCB
監測的決定性技術，但已收集和評估了目前採用的方法。即使是 NPP
使用的新一代電子產品，目前的電子產品中也並未採用系統層級和電路板層級診斷問題設計。電路板層級評估仍是一個不小的挑戰。

關鍵字

印刷電路板 (PCB)
儀錶和控制 (I&C)
診斷
測試
維護

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核电厂维护应用中心：印刷电路板诊断技术评估

1018534

总结报告 2009 年 3 月’

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报告摘要

本项目评估了先前 EPRI 印刷电路板 (PCB)
报告中的技术、理论方法和所提建议，旨在找到有助于延长 PCB 寿命的技术。

背景

核电厂 (NPP) 使用的印刷电路板 (PCB) 出自不同厂商，结构也各不相同。电厂使用的 PCB 在不断老化，故障次数也随之增加。所有 NPP 都有管理设备（包括 PCB）性能的政策和维护计划。PCB 维护计划的重要性因其与电厂安全和运行的关系而异。

仪表和控制 (I&C) 人员对于 PCB 的结构和使用非常熟悉，但他们有可能不太熟悉电路板层级的故障机制和部件故障。电力科学研究院 (EPRI) 进行了若干项调查，努力开发监测 PCB 性能的方法，以在发生故障前对电路板进行检测。本项目评估了先前 EPRI 报告中的技术、理论方法和所提建议，重点讨论以下两种方法：

- 确定可以用于监测单个部件退化的技术
- 确定可以开发用于监测电路板和系统性能的理论方法和技术

目的

- 评估用于检测 PCB 状况的现有诊断技术
- 确认所建议技术的能力和局限性，及其是否能够在线或离线确定电路板故障先兆
- 包括现场试验证明方法、其使用简易性、设备成本及供应状况

方法

本项目采用以下方法：

1. 首先，为确定在核电业以及其他行业中使用的经过证明的技术和诊断技术，对先前的 EPRI 调查进行评估。
2. 调查 PCB 部件故障的性质。
3. 针对技术选择，制定评估标准。
4. 对商业测试设备和技术进行审核。
5. 对本行业进行调查，确定预防性维护计划应采用的方法和诊断技术。
6. 对其他行业的诊断技术进行调查，找出管理 PCB 寿命周期的最新方法。
7. 审核各项技术确认故障和故障先兆的能力。

结果

本项目得出以下结果：

- PCB 故障随机发生。有些随机故障与老化有关，因此可以监测出 PCB 退化情况，而有些故障不可预测，可随时都可能发生。随着制造工艺质量的改善，与老化有关的不可预测故障的次数有所减少。
- 要监测出 PCB 所有故障模式是不可能的。已采用军事、航空和汽车行业所采用的方法来确定薄弱环节部件，并以此为基础建立了维护计划。
- 找出新方法来判断更换电路板的时间，即剩余寿命分析，该方法广泛应用于军事、航空和汽车行业。
- 军事、航空和汽车行业正通过预测学和健康状况管理计划来解决此问题。此方法广泛应用于 F-22，并且越来越多地用于机载航空电子设备和汽车电子系统方面。最终目标是让健康状况自动管理计算机监测诊断（与技术规范不符的条件）和环境条件。这样会减少外部测试的需求。

- 建议采用一系列经过证明的诊断技术。目前美国核电厂只使用了其中部分技术，因此可以用于增强电厂 PCB 预防性维护计划。

EPRI 远景

本项目着手完成先前 EPRI 报告中开始的工作，旨在开发出一套可以很方便地用于监测 PCB 状况的诊断技术。

尽管评估结果并未得出 PCB
监测的决定性技术，但对目前采用的方法进行了收集和评估。即使是 NPP
使用的新一代电子产品，目前的电子产品中也并未采用系统层级和电路板层级诊断问题设计。电路板层级评估仍是一个不小的挑战。

关键词

印刷电路板 (PCB)
仪表和控制 (I&C)
诊断
测试
维护

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REFERENCES

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Ce rapport décrit une recherche effectuée sous l'égide de l'Electric Power Research Institute (EPRI - Institut de recherche sur l'énergie électrique).

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Centre d'applications de maintenance nucléaire : Évaluation des techniques de diagnostic de circuits imprimés. EPRI, Palo Alto (Californie), États-Unis : 2009. 1018534.

SOMMAIRE DU RAPPORT

Ce projet a évalué les techniques, méthodes théoriques et recommandations faites par les rapports EPRI précédents sur les circuits imprimés. L'objectif était de trouver des techniques pour aider à gérer la vie des circuits imprimés.

Historique

Les circuits imprimés dans les centrales nucléaires proviennent d'une grande variété de fabricants et présentent divers types de construction. Les circuits imprimés vieillissent dans les centrales et plus les composants sont vieux, plus ils sont défaillants. Toutes les centrales nucléaires présentent des programmes de maintenance et des politiques pour gérer la performance de l'équipement, y compris celle des circuits imprimés. Les programmes de maintenance diffèrent au niveau de l'importance accordée aux circuits imprimés selon leur rôle au niveau de l'exploitation et de la sécurité des centrales.

Le personnel d'instrumentation et de commande est familier avec la construction et le fonctionnement des circuits imprimés, mais peut l'être moins avec les mécanismes de défaillance au niveau du circuit et des composants. EPRI a entrepris plusieurs recherches afin de développer des méthodes de surveillance de la performance des circuits imprimés pour détecter les circuits défectueux avant leur défaillance. Ce projet a évalué les techniques, méthodes théoriques et recommandations faites par les rapports EPRI précédents, en centrant les efforts sur deux approches :

- Identifier les techniques qui peuvent être utilisées pour surveiller la dégradation des composants individuels
- Identifier les méthodes théoriques et les techniques qui peuvent être développées pour surveiller la performance des systèmes et des circuits

Objectifs

- Évaluer les techniques de diagnostic existantes et la technologie utilisée pour estimer l'état des circuits imprimés
- Identifier les capacités et les limites des techniques recommandées, leur capacité à identifier les précurseurs de défaillance de circuit, ainsi que leur capacité à être utilisées en ligne et hors ligne
- Inclure des preuves sur le terrain des méthodes, de leur facilité d'emploi, de leur coût, et de la disponibilité de l'équipement

Approche

Ce projet a adopté l'approche suivante :

1. Tout d'abord, une évaluation a été faite à partir des recherches précédentes d'EPRI pour identifier les technologies et techniques de diagnostic éprouvées en vigueur dans les industries nucléaires et autres.
2. La nature des défaillances de composants de circuits imprimés a fait l'objet d'une recherche.
3. Des critères d'évaluation ont été établis pour la sélection de techniques.
4. Une revue des techniques et équipements de test du commerce a été menée.
5. L'industrie a fait l'objet d'une enquête pour déterminer quelles approches et techniques de diagnostic étaient utilisées pour les programmes de maintenance préventive.
6. Les techniques de diagnostic dans les autres industries ont fait l'objet de recherche des toutes dernières approches de gestion des cycles de vie de circuits imprimés.
7. Chaque technique a été passée en revue pour sa capacité à identifier les défaillances et les précurseurs de défaillance.

Résultats

Ce projet a abouti aux résultats suivants :

- Les défaillances de circuit imprimé se produisent de manière aléatoire. Certaines défaillances aléatoires sont associées au vieillissement, ce type de dégradation peut donc être surveillé, alors que d'autres sont imprévisibles et peuvent survenir à tout moment. Alors que la qualité des processus de fabrication s'améliore, le nombre de défaillances imprévisibles liées au vieillissement diminue.
- La surveillance de tous les mécanismes de défaillance sur un circuit imprimé est impossible. L'approche adoptée dans les industries militaires, aérospatiales et automobiles a été d'identifier les composants présentant la plus grande faiblesse et de définir un programme de maintenance en fonction de ceux-ci.
- Une nouvelle approche a été identifiée pour déterminer le moment de remplacement d'un circuit, en utilisant l'analyse de vie restante, ce qui est très utilisé dans les industries militaires, aérospatiales et automobiles.
- Les industries militaires, aérospatiales et automobiles approchent ce problème par un programme de gestion de santé et de pronostics. Ceci est considérablement utilisé sur le F-22 et est de plus en plus utilisé dans les systèmes électroniques de l'automobile et de l'avionique. L'objectif ultime est de faire surveiller les diagnostics (conditions en dehors des spécifications) et les conditions d'environnement par un ordinateur de gestion de santé autonome. Ceci éliminerait le besoin d'essais externes.
- Une série de techniques de diagnostic éprouvées a été recommandée. Ces techniques ne sont pas toutes actuellement utilisées dans les centrales nucléaires aux Etats-Unis et peuvent donc être utilisées pour améliorer le programme de maintenance préventive des centrales pour les circuits imprimés.

Point de vue de l'EPRI

Le projet a été entrepris pour compléter le travail commencé dans les rapports EPRI précédents, avec l'objectif de développer un ensemble de techniques de diagnostic qui peuvent être immédiatement utilisées pour surveiller les conditions des circuits imprimés.

Bien que les résultats de l'évaluation n'aient pas donné de techniques conclusives pour la surveillance des circuits imprimés, les méthodes actuellement en vigueur ont été recueillies et évaluées. Les problèmes de diagnostics au niveau des circuits et des systèmes n'ont pas été conçus dans l'électronique actuelle, même pour la nouvelle génération d'électronique utilisée dans les centrales nucléaires. Les évaluations au niveau du circuit restent très difficiles.

Mots-clés

Circuit imprimé
Instrumentation et commande
Diagnostics
Essais
Maintenance

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原子力保全アプリケーションセンター：プリント基板における診断技術の評価

1018534

2009年3月最終レポート

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*原子力保全アプリケーションセンター：*プリント基板における診断技術の評価EPRI, Palo Alto, CA: 2009. 1018534.

レポート概要

このレポートは、プリント基板 (PCB) について以前の EPRI
レポートに含まれる技術、理論的方法、および推奨事項を評価しました。このレポートの目的は、プリント基板の寿命を管理する技術を見つけることでした。

背景

原子力発電所 (NPP) におけるプリント基板(PCB)
のメーカーとその製品は多岐にわたっています。プリント基板
は発電所内でエージングが進みつつあり、機器の高経年化に伴い、故障の回数も増加しています。すべての 原子力発電所
で、プリント基板を含む機器のパフォーマンス管理のための規定と保全プログラムが設けられています。当該のプリント基板の発電所の安全と運転に対する重要度に応じ、保全プログラムはそれぞれ異なります。

計測制御 (I&C) の技術者は、プリント基板
の構成と動作については詳しいものの、基板レベルでの故障メカニズムや部品の故障について熟知していない可能性があります。Electric Power Research Institute (EPRI)
では、故障前の基板の欠陥を検出するためプリント基板の
パフォーマンスの監視方法を開発するために、いくつかの調査を行いました。このプロジェクトは、2
つのアプローチに焦点を当て、以前のEPRIレポートに含まれる技術、理論的方法、推奨事項を評価しました。

- 個々の機器の劣化の監視に使用できる技術の特定
- 基板とシステムのパフォーマンスを監視するために開発の可能性のある理論的方法と技術の特定

目的

- PCB の状態評価のために使用されている既存の診断手法と技術を評価すること
- 推奨された技術について，基板故障の前兆の特定能力と運転中保全または定検中保全での実施能力の観点から，その技術の能力と限界の特定を行うこと、
- 方法に関しての発電所での裏付け、使いやすさ、コスト、機器のアベイラビリティを含めること

アプローチ

このプロジェクトで使用したアプローチは以下のとおりです。

1. まず初めに、原子力およびその他の産業界で使用されている、実績のある技術と診断技術を特定するため、過去の EPRI の調査を評価。
2. プリント基板機器の故障の性質を調査。
3. 技術の選択のための評価クライテリアを確立。
4. 市販されている試験装置と技術のレビューを実施。
5. 予防保全プログラムでどのアプローチと診断技術が使用されているかを決定するために、産業界での調査を実施。
6. プリント基板
   のライフサイクル管理に対する最新のアプローチを知るために、その他の産業界での診断技術を調査。
7. 故障とその前兆の特定能力について、それぞれの技術をレビュー。

結果

このプロジェクトで得られた結果は以下のとおりです。

- プリント基板
  故障は、ランダムに発生します。いくつかのランダムな故障はエージングに関係するものであるため、その劣化を監視することができますが、その他の故障は予測不可能であり、常に故障の可能性があります。製造プロセスの品質の向上に伴い、予測不可能な高経年化に関する故障の数は減少します。

- プリント基板
  に関するすべての故障メカニズムを監視することは不可能です。軍事、航空産業界、および自動車産業界により取られているアプローチは、最も弱い(ウィークリンク)機器を特定し、それらの機器について保全プログラムを設定するためのものでした。
- 軍事、航空産業界、および自動車産業界で幅広く使用されている余寿命分析を使用した、基板の交換の時期を決定するための新しいアプローチが特定されました。
- 軍事、航空産業界、および自動車産業界は、予測と健全性管理プログラムを通して、この問題に取り組んでいます。これは、F-22で広範囲にわたり使用され、飛行機の航空電子工学や自動車の電子システムで更なる使用がみられます。最終的な目的は、自立した健全性管理コンピュータに仕様外条件の診断と環境の状態を監視してもらうことにあります。これにより、外部試験の必要性が除外されます。
- 一連の実績のある診断技術が推奨されました。これらの技術は、米国の原子力発電所ですべて現在使用されていないため、発電所の プリント基板
  の予防保全プログラムを強化するために使用することができます。

EPRIの観点

このプロジェクトは、プリント基板
状態の監視のためにすぐに使用できる診断技術の開発を目的として、過去の EPRI レポートで開始された作業を完了するために行われました。

評価の結果から プリント基板
監視のための決定的な技術は導き出されませんでしたが、現在使用されている方法の収集と評価は行われました。システムレベルおよび基板レベルでの診断に関する問題は、原子力発電所
で使用されている新世代の電子機器であっても、現在の電子機器の設計に組み込まれていないことでした。それらは基板レベルでの評価には、課題が残されています。

キーワード

プリント基板 (PCB)

計測および制御 (I&C)

診断

試験

保全

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원자력 보수 응용 센터(Nuclear Maintenance Applications Center): 인쇄 회로 기판 진단 기술 평가

1018534

최종 보고서, 2009년 3월

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(B) 본 문서 또는 모든 정보, 기구, 방법, 절차 또는 본 문서에 공개된 유사한 항목을 사용자가 선택하거나 사용함으로 인해 발생하는 기타 모든 손상이나 책임(EPRI 또는 EPRI 대표자가 인과적 손상의 가능성을 알린 경우를 포함하여 모든 인과적 손상을 포함)에 대한 책임을 가정.

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이 보고서는 다음의 방식으로 문헌에서 인용된 기업 문서입니다:

원자력 보수 응용 센터(Nuclear Maintenance Applications Center): Assessment of Printed Circuit Board Diagnostic Techniques(인쇄 회로 기판 진단 기술 평가). EPRI, Palo Alto, CA: 2009. 1018534.

보고서 요약

이 프로젝트에서는 인쇄 회로 기판(PCB)에 대한 이전 EPRI 보고서의 기술, 이론적 방법, 권장사항을 평가했습니다. 평가 목표는 PCB 수명을 관리하는 기술을 연구하는 것이었습니다.

배경

원자력 발전소(NPP)의 인쇄 회로 기판(PCB)의 제조업체와 구조는 다양하게 있습니다. 부품과 마찬가지로 PCB는 발전소에서 노화되면서 오류 횟수도 증가합니다. 모든 NPP에는 PCB와 같은 장비의 성능을 관리하기 위한 규정 및 유지관리 프로그램이 있습니다. 유지관리 프로그램은 발전소 안전 및 운영과의 관계에 따라 PCB에 적용되는 중요성이 다양합니다.

계측 및 제어(I&C) 직원들은 PCB의 구조 및 작동에 대해 잘 알고 있지만 기판 차원의 오류 메커니즘 및 구성요소 고장에 대해서는 잘 모를 수 있습니다. EPRI(Electric Power Research Institute)는 오류가 발생하기 전에 기판을 파악하기 위해 PCB 성능을 모니터링하는 방법을 개발하기 위한 노력으로 몇 가지 조사를 실시했습니다. 이 프로젝트에서는 다음의 두 가지 접근방법에 초점을 맞추어 이전 EPRI 보고서의 기술, 이론적 방법, 권장사항을 평가했습니다.

- 개별 구성요소의 성능 저하를 모니터링하기 위해 사용할 수 있는 기술 파악
- 기판 및 시스템 성능을 모니터링하기 위해 개발할 수 있는 이론적 방법 및 기술을 식별

목표

- 기존의 진단적 기술과 PCB 상태를 평가하기 위해 사용하는 기술의 평가
- 권장 기술의 기능 및 제한 사항을 식별하고 기판 오류의 징후를 감지하고 온라인 또는 오프라인 상태에서 업무를 수행하는 능력을 파악

- 방법, 사용의 간편성, 비용, 장비 가용성 등에 대한 현장 검증을 포함

접근방법

이 프로젝트에서는 다음의 접근방법을 사용했습니다:

1. 우선, 원자력 및 기타 업계에서 사용하는 입증된 기술 및 진단 기술을 식별하기 위해 이전 EPRI 조사에 대해 평가했습니다.
2. PCB 구성요소의 특성에 대해 조사했습니다.
3. 기술 선택을 위한 평가 기준을 마련했습니다.
4. 상용 테스트 장비 및 기술에 대한 평가를 실시했습니다.
5. 업계에서는 예방 유지관리 프로그램을 위해 사용한 접근방법 및 진단 기술을 확인하기 위한 설문조사를 실시했습니다.
6. PCB 수명 주기를 관리하기 위한 최신 접근방법을 알아보기 위해 다른 업계에서의 진단 기술을 조사했습니다.
7. 오류 및 오류의 징조를 식별할 수 있는 능력에 대해 각각의 기술을 검토했습니다.

결과

이 프로젝트에서는 다음의 결과를 얻었습니다:

- PCB 오류는 임의적으로 발생합니다. 일부 임의적 오류는 노화와 관련이 있을 수 있으므로 성능 저하를 모니터링할 수 있으며 일부 오류는 예측이 가능하며 언제든지 오류가 발생할 수 있습니다. 제조 공정의 품질이 개선되면서 예측 불가능한 노화 관련 오류도 감소합니다.
- PCB의 모든 오류 메커니즘을 모니터링하는 것은 불가능합니다. 군대, 항공 우주, 자동차 업계에서 선택한 접근방법으로 취약부(weak-link) 구성요소를 식별하고 이에 대한 유지관리 프로그램의 기초를 수립했습니다.
- 잔여 수명 분석을 사용한 기판 교체 시기 결정을 위해 새로운 접근방법을 찾아 군대, 항공 우주, 자동차 업계에서 광범위하게 사용하고 있습니다.
- 군대, 항공 우주, 자동자 업계는 예비 진단 및 보건 관리 프로그램을 통해 이 문제에 접근하고 있습니다. 이것은 F-22에서 확장적으로 사용되며 항공 전자기기 및 자동차

전자 시스템에서의 사용이 증가하고 있습니다. 궁극적인 목표는 자치적인 보건 관리 컴퓨터가 진단(기준 일탈 상태) 및 환경 상태를 모니터링하도록 하는 것입니다. 이로써 외부 테스트의 필요성이 없어질 것입니다.

- 일련의 입증된 진단 기술을 추천 받았습니다. 이러한 기술은 현재 미국의 모든 원자력 발전소에서 현재 사용하고 있지 않으며 발전소의 PCB 예방 유지관리 프로그램을 개선하기 위해 사용할 수 있습니다.

EPRI 관점

이 프로젝트는 이전 EPRI 보고서에서 완료될 예정이었으며 PCB 상태를 모니터링하기 위해 즉시 사용할 수 있는 일련의 진단 기술을 개발하는 것이 목표였습니다.

평가 결과 PCB 모니터링을 위한 결론적인 기술을 찾지는 못했지만 현재 사용하는 방법을 수집하고 평가할 수 있었습니다.. 시스템 및 기판 차원의 진단 문제는 NPP에서 새로운 세대의 전자기기를 사용하고 있지만 최신 전자기기로 설계하지 못한다는 것이었습니다. 기판 차원의 평가는 과제로서 남아 있습니다.

키워드

Printed circuit board(인쇄 회로 기판: PCB)

Instrumentation and control(계측 및 제어: I&C)

Diagnostics(진단)

Testing(테스트)

Maintenance(유지관리)

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Centro de aplicações de manutenção nuclear (Nuclear Maintenance Applications Center): avaliação das técnicas de diagnóstico de placas de circuito impresso

1018534

Relatório final, março de 2009

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RESUMO DO RELATÓRIO

Este projeto avaliou as técnicas, os métodos teóricos e as recomendações feitas em relatórios anteriores do EPRI sobre placas de circuito impresso (PCBs). O objetivo era encontrar técnicas para auxiliar no gerenciamento da vida útil dos PCBs.

Histórico

As placas de circuito impresso (PCBs) em usinas de energia nuclear (NPPs - nuclear power plants) são fabricadas por diversas empresas. Essas placas estão envelhecendo nas usinas e, à medida que seus componentes envelhecem, aumenta o número de falhas. Todas as NPPs possuem normas e programas de manutenção para administrar o desempenho de equipamentos, incluindo as PCBs. A importância dada às PCBs nos programas de manutenção está diretamente relacionada à segurança e operação da usina.

O pessoal de instrumentação e controle (I&C) está familiarizado com a fabricação e operação das PCBs, mas pode estar menos familiarizado com os mecanismos de falha da placa e dos componentes. O Instituto de Pesquisa de Energia Elétrica (EPRI) realizou diversas pesquisas na tentativa de desenvolver métodos de monitoramento do desempenho das PCBs para detectar as placas antes da falha. Esse projeto avaliou as técnicas, os métodos teóricos e as recomendações apresentadas em relatórios anteriores do EPRI, concentrando-se em duas metodologias:

- Identificar técnicas que poderiam ser usadas para monitorar a degradação de componentes individuais
- Identificar métodos teóricos e técnicas que poderiam ser desenvolvidas para monitorar a placa e o desempenho do sistema

Objetivos

- Avaliar as técnicas de diagnóstico existentes e a tecnologia usada para avaliar a condição das PCBs
- Identificar as capacidades e limitações das técnicas recomendadas e sua capacidade de identificar precursores da falha e de ser realizada on-line ou off-line.
- Incluir prova de campo dos métodos, sua facilidade de uso, custo e disponibilidade dos equipamentos

Metodologia

O projeto usou a seguinte metodologia:

1. Foi feita inicialmente uma avaliação das pesquisas anteriores do EPRI para identificar tecnologias e técnicas de diagnóstico comprovadas, atualmente empregadas no setor nuclear e em outros setores.
2. Pesquisou-se a natureza das falhas dos componentes das PCBs.
3. Foram estabelecidos critérios para a seleção das técnicas.
4. Realizou-se um exame das técnicas e dos equipamentos de teste disponíveis comercialmente.
5. Fez-se um levantamento do setor para estabelecer as metodologias e as técnicas de diagnóstico usadas para os programas de manutenção preventiva.
6. Pesquisaram-se as técnicas de diagnóstico em outros setores quanto às metodologias mais modernas para administrar os ciclos de vida útil das PCBs.
7. Cada técnica foi examinada quanto a sua capacidade de identificar falhas e precursores de falha.

Resultados

O projeto produziu os seguintes resultados:

- As falhas das PCBs ocorrem aleatoriamente. Algumas falhas aleatórias estão relacionadas à idade, de forma que sua degradação pode ser monitorada, ao passo que outras são imprevisíveis e podem ocorrer a qualquer momento. À medida que se aperfeiçoam os processos de fabricação, reduz o número de falhas imprevisíveis relacionadas à idade.
- É impossível monitorar todos os mecanismos de falha de uma PCB. A metodologia empregada nos setores militar, aeroespacial e automotivo tem sido a de identificar os componentes críticos e basear o programa de manutenção nesses componentes.
- Foi identificada uma nova metodologia para estabelecer quando a placa deve ser substituída, utilizando a análise de vida útil restante que é muito usada nos setores militar, aeroespacial e automotivo.
- Esses setores tratam desse problema através de um programa de prognósticos e gestão de saúde. Isso é usado amplamente no F-22 e cada vez mais na aviônica das aeronaves e sistemas eletrônicos automotivos. O objetivo final é ter um computador de gestão de saúde autônomo para monitorar os diagnósticos (as condições fora das especificações) e condições ambientais. Isso eliminaria a necessidade de testes externos.
- Foi recomendada uma série de técnicas de diagnóstico comprovadas. Nem todas essas técnicas estão sendo usadas em usinas nucleares nos Estados Unidos e, portanto, podem ser usadas para melhorar o programa de manutenção preventiva das PCBs da usina.

Perspectiva do EPRI

O projeto tinha como objetivo concluir o trabalho iniciado nos relatórios anteriores do EPRI, com o objetivo de desenvolver um conjunto de técnicas de diagnóstico que poderiam ser prontamente usadas para monitorar as condições das PCBs.

Embora os resultados da avaliação não tenham produzido técnicas conclusivas para esse monitoramento, os métodos usados atualmente foram compilados e avaliados. Os problemas de diagnósticos a nível de sistema e de placa não foram projetados na eletrônica atual, mesmo com a nova geração de sistemas eletrônicos usados em usinas de energia nuclear. A avaliação das placas continua sendo um desafio.

Palavras-chave
Placa de circuito impresso (PCB)
Instrumentação e controle (I&C)
Diagnóstico
Testes
Manutenção

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En este informe se describe la investigación patrocinada por el Instituto de Investigación de Energía Eléctrica (EPRI).

El informe es un documento corporativo que debe citarse en la literatura en el siguiente formato:

Centro de Aplicaciones de Mantenimiento Nuclear: Evaluación de las Técnicas de Diagnóstico de Circuitos Impresos EPRI, Palo Alto, CA: 2009. 1018534.

RESUMEN DEL INFORME

En este proyecto se evaluaron las técnicas, métodos teóricos y recomendaciones hechas por EPRI en informes anteriores acerca de circuitos impresos (PCBs). El objetivo consistía en encontrar técnicas para ayudar en la gestión del ciclo de vida útil de una PCB.

Antecedentes

Las PCBs usadas en las plantas de energía nuclear , son fabricadas por muchas entidades diferentes y de diversas formas. Las PCBs de las plantas están envejeciendo, y a medida que envejecen sus componentes, aumenta la cantidad de fallos de los mismos. Todas las tienen normas y programas de mantenimiento para la gestión del rendimiento del equipamiento, incluidas las PCBs. Los programas de mantenimiento difieren en la importancia que se da a las PCB en función de su relación a la seguridad y la operación de la planta.

Es posible que el personal de instrumentación y control (I&C) conoce la estructura y la operación de las PCBs, pero quizá no conozca muy bien los mecanismos de los fallos a nivel de la placa, y los fallos de los componentes. El Instituto de Investigación de Energía Eléctrica (EPRI) llevó a cabo varias investigaciones con el fin de desarrollar métodos de control del rendimiento de las PCBs para detectar las placas defectuosas antes de que fallen. En este proyecto se evaluaron las técnicas, métodos teóricos y recomendaciones hechas en informes anteriores de EPRI, centrándose en dos enfoques:

- Identificar las técnicas que podrían utilizarse para monitorizar la degradación de los componentes individuales
- Identificar los métodos teóricos y las técnicas que podrían desarrollarse para monitorizar el rendimiento de la placa y del sistema

Objetivos

- Evaluar las técnicas actuales de diagnóstico y la tecnología utilizada para evaluar la condición de las PCBs
- Identificar las capacidades y las limitaciones de las técnicas recomendadas y su capacidad para identificar los factores que anteceden al fallo de la placa, y de aplicarse tanto en línea como fuera de línea
- Incluir ensayo de la aplicación en el campo de tales métodos, el grado de facilidad de su uso, el coste y la disponibilidad de equipos

Enfoque

En este proyecto se utilizó el siguiente enfoque:

1. Primero, se hizo una evaluación de previas investigaciones hechas por EPRI para identificar las tecnologías comprobadas y las técnicas de diagnóstico utilizadas tanto en la industria nuclear como en otros sectores.
2. Se investigó la naturaleza de los fallos de los componentes de las PCBs.
3. Se establecieron criterios de evaluación para la selección de técnicas.
4. Se examinaron los equipos y las técnicas de ensayos disponibles a nivel comercial.
5. Se hizo una encuesta del sector para determinar cuáles enfoques y técnicas de diagnóstico estaban utilizándose en los programas de mantenimiento preventivo.
6. Se investigaron las técnicas de diagnóstico en otras industrias para determinar los últimos métodos de manejo de los ciclos de vida útil de las PCBs.
7. Se examinó la capacidad de cada técnica de identificar los fallos y los precursores que les anteceden.

Resultados

En este proyecto se obtuvieron los siguientes resultados:

- Los fallos de las PCBs ocurren de forma aleatoria. Algunos fallos aleatorios se relacionan con la antigüedad de las placas, por lo cual es posible monitorizar su degradación, mientras que otros son imprevisibles y pueden ocurrir en cualquier momento. A medida que mejora la calidad de los procesos de fabricación, se reduce la cantidad de fallos imprevisibles que se atribuyen a la antigüedad.
- Es imposible monitorizar todos los mecanismos de fallo de una PCB. El método utilizado en los sectores militares, aeroespaciales y automotrices ha consistido en la identificación de los enlaces débiles entre los componentes basando un programa de mantenimiento en torno a éstos.
- Se identificó un nuevo método para determinar el momento de reemplazar una placa mediante el análisis de la vida útil restante de la misma, método que se utiliza ampliamente en las industrias militares, aeroespaciales y automotrices.
- Las industrias militares, aeroespaciales y automotrices enfrentan este problema mediante un programa de pronóstico y gestión de salud. Se utiliza ampliamente en el F-22, y cada vez más en aviones y sistemas electrónicos automovilísticos. El objetivo final consiste en hacer que un ordenador autónomo de gestión de salud monitorice el diagnóstico (condiciones fuera de especificación) y las condiciones ambientales. Así se eliminaría la necesidad de realizar ensayos externos.
- Se ha recomendado una serie de técnicas comprobadas de diagnóstico. No todas estas técnicas se usan actualmente en las plantas nucleares de Estados Unidos y por tanto pueden utilizarse para mejorar el programa de mantenimiento preventivo para las PCBs en una planta.

La perspectiva de EPRI

Con el proyecto se buscaba concluir el trabajo que se inició en informes previos de EPRI cuyo objetivo era desarrollar un conjunto de técnicas de diagnóstico que pudieran utilizarse inmediatamente para monitorizar las condiciones de las PCBs.

Aunque los resultados de la evaluación no arrojaron técnicas definitivas para la monitorización de las PCBs, se han reunido y evaluado los métodos utilizados en la actualidad. Los problemas del diagnóstico a nivel de sistema y de placa no han sido incluidos en laelectrónica actuale, como tampoco en la nueva generación de la electrónica utilizada en las NPPs. Las evaluaciones a nivel de placa siguen siendo un reto.

Palabras clave

Placa de Circuito Impreso (PCB)
Instrumentación y control (I&C)
Diagnóstico
Ensayos
Mantenimiento

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