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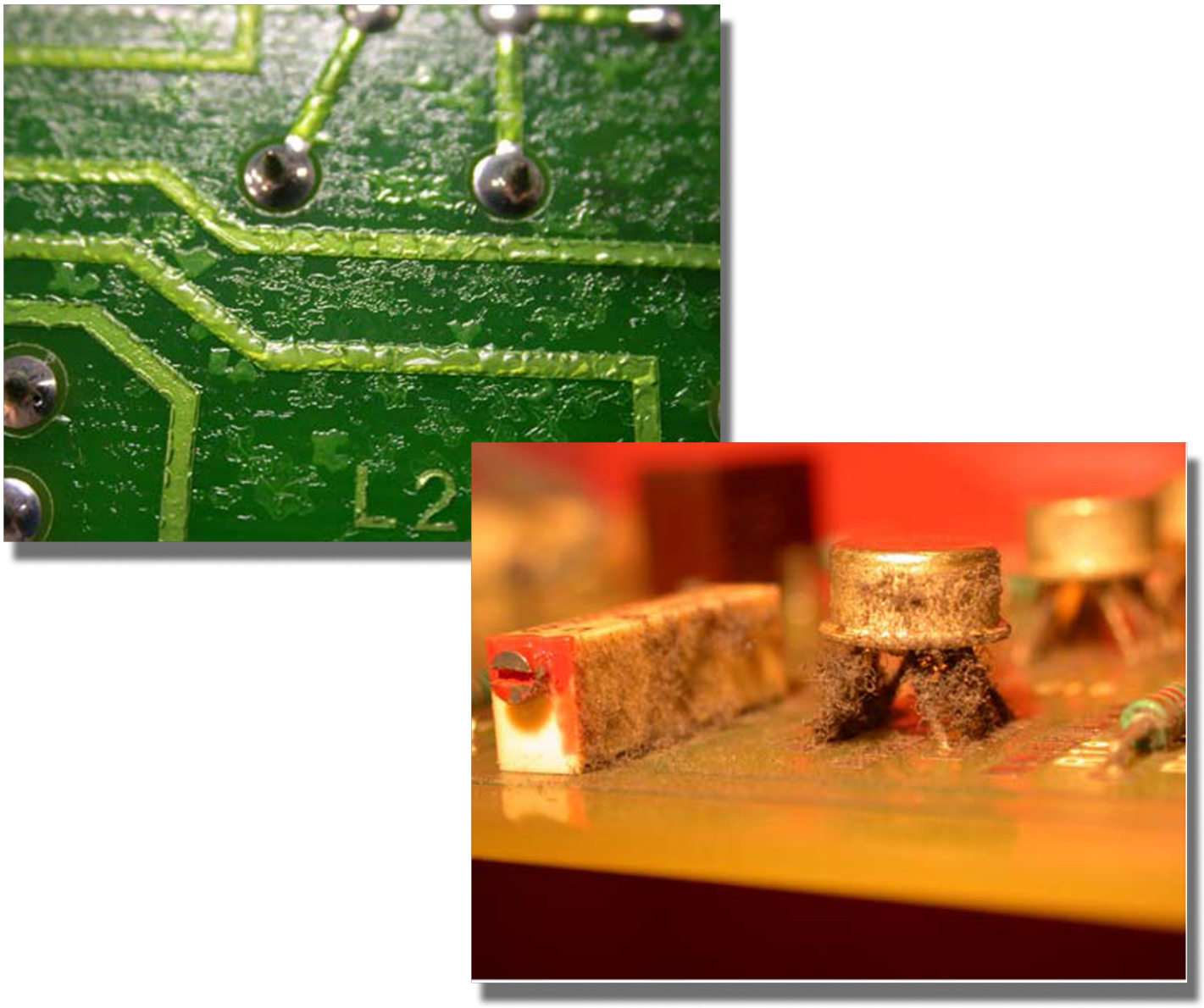
Guidance for Aging Management of Instrumentation and Control (I&C) Circuit Cards and Components Based on Électricité de France (EDF) Experience



Guidance for Aging Management of Instrumentation and Control (I&C) Circuit Cards and Components Based on Électricité de France (EDF) Experience

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Final Report, November 2010

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ABSTRACT

This report deals with the good practices recommended by Electricité de France (EDF) Research & Development (R&D) concerning the maintenance of Printed Circuit Boards (PCB) used in nuclear power plants. It is shown than the procedure developed by EDF R&D is mainly based on visual inspection and deep physical analysis (destructive analysis of components and PCB) in order to evaluate the aging of a PCB. Some specific tools (dedicated to the aging evaluation of electronic components such as capacitors, optoelectronic couplers, thyristors and other power components) can be developed and are described here. When the aging status is determined, it is then possible to define critical electronic components and/or boards. The aging of these boards has to be carefully followed and when necessary preventive maintenance can be performed. Some examples of this are given.

Finally this report discusses some ideas in order to mitigate the stressors that may affect the remaining life-time of PCBs. The main stressors discussed are handling (including electrostatic discharges), environment conditions (pollution, temperature, humidity) and electrical overloads. For each stressor some good practices are given. A special focus is made on storage conditions.

REPORT SUMMARY

Circuit cards of instrumentation and control (I&C) systems in nuclear power plants are designed for several decades of use and are inevitably subject to aging. Aging can result in the appearance of numerous failures, or it may lead to a drift of the electrical properties of a component, which can have different levels of critical consequences depending upon the systems concerned. The risk of such failures increases with circuit card age. Described here are several good practices to inspect for aging effects and to mitigate external factors that lead to premature aging of circuit cards and their components.

Background

Circuit card failures are a significant contributor to nuclear power plant forced outages and system failures, leading to undesirable plant transients and reduced power operation levels. These failures cost the nuclear power industry many millions of dollars annually due to lost revenue, replacement power purchases, increased labor, and unnecessary challenges to plant safety systems. Aging issues are raising serious concerns that the number of forced outages and system failures caused by circuit cards and their components will increase significantly over the life of the plant.

Operating nuclear power plant owners are expecting longer lifetimes with high reliability from existing I&C systems. An understanding of circuit card aging is critical to achieving such expectations. The anticipation of failures of I&C systems and the decision for refurbishing or reengineering a system are directly related to the consequences associated with aging of circuit cards and components. An appropriate monitoring of aging, therefore, allows for an optimized maintenance policy and, in the end, for an extension of I&C system life expectancy. This report identifies approaches to better understand aging of circuit card components and to use that knowledge to better assess their remaining useful life.

Objective

To provide good practices and other valuable information based upon observations and analyses of circuit card and component aging effects on Électricité de France (EDF) plants.

Approach

The project team reviewed information supported by observations of a few thousand failed and abnormal circuit cards and components from EDF fleets of 30 900-MWe and 20 1300-MWe nuclear power plants. The team applied the information from these observations to gain important insight on the aging of circuit cards and their components. Based on this review, the team identified good practices for aging inspections and monitoring as well as limiting of external factors that contribute to aging.

Results

Visual inspection is a valuable tool to understand the current state of the circuit card and its components. This report provides guidance on the appropriate order of inspections, required tools and criteria for inspections, limitations of visual inspections, and examples of defects. In order to gain more detailed understanding of the aging of circuit cards and components, nondestructive off-line testing approaches as well as destructive techniques are discussed.

The report provides guidance on analyzing results from visual, nondestructive, and destructive techniques to develop assessments of the aging of circuit cards and components. Such assessments can be used to establish lists of components that are sensitive to aging and components that are not likely to reach their expected useful life. Once sensitive components are identified and the causes and rates of operational failures are known, it is possible to set up an effective policy of judicious preventive replacement to limit the number of failures.

The results of this report can be used by utilities to increase their understanding of aging mechanisms and the attendant consequences based on plant operating experience. The good practices can also be used to modify plant procedures and practices in order to help reduce external factors that contribute to aging. Finally, the tools and techniques for monitoring, analysis, and prediction of aging can be used to improve maintenance practices and thereby extend the life of circuit cards and the I&C systems that rely on them.

EPRI Perspective

EDF and EPRI have documented considerable circuit card failure and aging operating experience. They have defined a set of good practices for assessing the aging of circuit cards and electronic components in two reports, available as a set under EPRI order number 1008166: *Collected Field Data on Electronic Part Failures and Aging in Nuclear Power Plant Instrumentation and Control (I&C) Systems* (EPRI report 1003568, 2002) and *Guidelines for the Monitoring of Aging of I&C Electronic Components* (1008166, 2004). The current report, 1022246, describes the results of more recent work; additional good practices will be presented in another report to be developed in 2011. Material from 1022246 will also be incorporated into an ongoing EPRI companion project to develop circuit card life-cycle management guidelines, slated for publication in 2011.

Keywords

Circuit Cards
Circuit Boards
Aging
Failure Analysis
Electronic Components
Reliability
Maintenance
Visual Inspection

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1
AGING AND LOSS OF RELIABILITY OF PRINTED CIRCUIT BOARDS

The printed circuit boards of instrumentation and control systems in nuclear power plants are designed to be used for several decades and are inevitably subject to aging. Despite being used in a relatively protected and stress-free environment, they are continuously subjected to external factors which will alter their electrical characteristics internally. Also inevitably and for fundamentally thermodynamic reasons (completely independent of the operator), electronic components, printed circuits, etc., will age, if only because of ambient temperature which, over period of 30 to 40 years, is no longer a negligible factor. Aging does not necessarily result in the appearance of numerous failures. It may simply lead to a drift of the electrical properties of a component (longer response time, reduction in the gain of a transistor, modification of the value of the capacitance of a capacitor, etc.) which are, depending on the systems concerned, more or less critical and more or less acceptable. Nevertheless, in all cases, the risk of failure increases with aging.

Although the fundamental causes of aging and loss of reliability are physical in nature, we must try to limit the effects of aging. Without being able to prevent printed circuit boards from aging, we shall try to slow aging as much as possible. This involves creating an appropriate policy on maintenance and MRO (maintain, repair and operation). Although based on a relatively old technology in general, the instrumentation and control systems of nuclear power plants remain potentially sensitive to aging if we include the time factor. For example, active components (e.g., thyristors, transistors) manufactured in the 1990s, provided that they were produced according to the state of the art of the time, are considered to have a life span of 50 years, or even more. These life spans, albeit long, roughly correspond to the life spans of nuclear plants. Therefore, while the aim is to extend the life span of instrumentation and control systems to match the entire life span of the plant, the margin between the theoretical life span of the component and its actual life may be quite small. That is why we should adopt a number of good practices to limit the attacks on printed circuit boards, be capable of assessing their aging (if only to know whether new practices should be defined, if the system has to be renovated, etc.).

Good practices are governed by a certain number of essentials. As mentioned above, their main aim is to limit any external factors and seek to extend the life span of equipment, while maintaining an optimum level of reliability. The good practices may be classified into three major groups: those concerning the monitoring of aging (types of analysis, frequency, etc.), those concerning taking account of such aging and, finally those concerning the mitigation of external factors.

The purpose of this report is to describe the good practices introduced by Electricité de France (EDF) and covers, in particular, the recommendations and techniques developed by EDF

Research and Development (R&D), which is responsible within EDF for the development of the methodologies and the definition of good practices.

Chapters 2 and 3 of this report describe good practices in terms of the inspection for and the monitoring of aging to assess the remaining useful life. Chapter 2 discusses visual inspections, which constitute one of the two main areas of research into aging. Chapter 3 concerns, among other things, additional means including a description of non destructive testing equipment for specific components and destructive testing, the second main aspect for obtaining a detailed knowledge of the state of aging.

Chapter 4 of this report discusses into the usefulness of a technology watch of operating experience in other industries and how to account for it in assessing remaining life.

Chapter 5 discusses establishing a detailed inventory of the components in instrumentation and control systems that are affected by aging and those that are likely to not meet their design life. There is given an approach to determine, based on the aging of electronic components, modules and even critical systems, which should be monitored in particular.

Chapter 6 discusses the possibility of limiting the impact of external factors on components, modules and systems previously shown to be sensitive to aging for all usual factors such as temperature, humidity, pollution, etc.

Finally, Chapter 7 reviews several aspects being developed to improve maintenance practices still further through better analysis and prediction of aging to find better approaches for maintaining operational conditions.

2
PERIODIC VISUAL INSPECTIONS OF PRINTED CIRCUIT BOARDS

General Principle

At EDF R&D, one of the two main aspects concerning the monitoring of the aging of the printed circuit boards of instrumentation and control systems lies in the analysis of direct visual inspection of printed circuit boards (PCB). The approach, which is applicable to all electronic circuit boards, consists in reviewing a series of criteria, which may be observed visually and reveal the state of aging of the electronic circuit board. In order to limit the inspection time, the observation should focus on points which, in the light of experience, the operator has decided are critical. The inspector reviews for abnormalities the following in the indicated order:

- Overall appearance of the printed circuit board.
- State of solders.
- Faults observed on components.
- Faults on connectors.

The following points should also be examined, depending on the components concerned and the history of the board:

- The state of any repairs.
- Specific visual inspection of relays.

Tools Required

The inspections described here are visual, but this does not mean that no special tools are required. For optimum results, it is useful to have the following equipment available:

- A 5 to 10 magnifier.
- One directional source and another circular source of white light.
- A source of ultra-violet light.
- A microscope with higher magnification, typically at least x 20.
- An endoscope with a small diameter (see Figure 2-1), capable of observations of the back of instrumentation and control system racks (capable of transmitting both white light and ultraviolet radiation).

- An IPC A 610 index D guide (latest version, incorporating RoHS assemblies). The standard IPC A 610 specifies the acceptance criteria for printed circuit boards leaving the assembly line. It comprises three levels of requirements: the first concerns domestic electronic consumer goods for which high reliability and long life span are not essential. On the other hand, class 3 is the most restrictive and is intended for application in safety-related, military applications, etc. The instrumentation and control system falls, quite naturally, into class 3. Nevertheless, some criteria may be used for class 2. EDF R&D uses this standard prior to the creation of its own frame of reference.

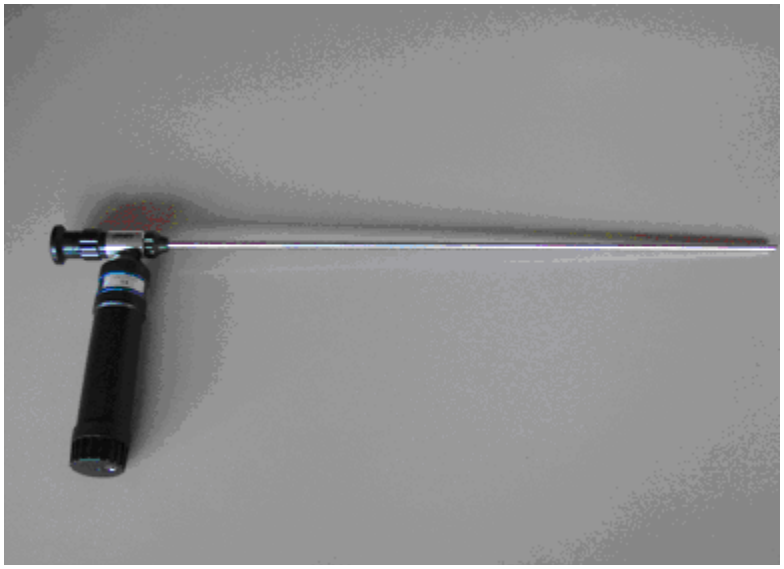

Figure 2-1
Endoscope used for inspections

We must be very cautious as to the level of magnification used during inspections (using a magnifier or microscope). Magnifications greater than x 10 should be used sparingly and only to confirm a fault (and not to find it). Relatively high levels of magnification may only be used to detect faults on highly integrated boards. Indeed, by magnifying a specific point, it is always possible to observe a fault. Let us take for example, the case of a solder. The acceptance criterion generally accepted for a tin-lead solder (Sn63Pb37) is that it should be smooth and shiny, as laid down in standard IPC A 610. Now magnification of x 10 or more is enough to reveal a granular surface appearance of solders, especially when they are made by hand. It is also easy to reveal the presence of cracks not visible to the naked eye. All these aspects may lead an inexperienced inspector to classify such solders as unsatisfactory or spend a long time checking whether all the minor faults observed comply with class 3 of standard IPC A 610 or not.

Criteria Assessed During Visual Inspection

Each of the main categories described above is then divided up into a large number of criteria, given in detail in the remainder of this chapter. Therefore, when checking the overall appearance of the printed circuit board, the PCB should be checked for the presence or lack of presence of the following:

- Overheating.
- Buckling of the board.
- Delamination or even cracking of the printed circuit.
- Severe accumulation of dust (leading, in particular, to a bridge of dust between two component pins, which may result in a short-circuit if the dust conducts).
- Deposition of unexpected particles.
- Residues of alloy used for solders outside the pads for solder paste.
- Integrity of the coat of varnish for tropicalized or varnished boards.
- Separation of tracks and mounting pads for electronic components.
- Oxidation or corrosion of the conductors on printed circuits (visible especially for copper tracks).
- Obvious design faults of printed circuit boards.

In so far as the **"state of solders"** is concerned, the criteria to be taken into consideration are as follows:

- Presence of dull solders (and, therefore, carried out badly).
- Presence of accidental alloy bridges between two solders.
- Quality of the solders (lack of solder, sufficient rise of the solder on the component, form of the soldered joint, etc.) according to standard IPC A 610 index D.

In the category **"faults observed on components"**, special attention should be paid to the following points:

- Presence of whiskers on the pins of components.
- Corrosion of the pins or casings of components.
- Signs of impact, cracking of casings (to be checked for hermetically sealed components).
- Overheating of components.
- Leaks of electrolyte from electrochemical capacitors.
- Components mounted incorrectly (particularly in terms of the earthquake qualification of heavy components which should be maintained by specific attachments).
- Pins of bent components.
- Tin plating on gold plated pins: making a solder on components with gold plated pins will lead to the formation of gold-based intermetallic compounds in the solder. If the gold content in the final solder is too high (1% may suffice), the solder will have a very short life span. If the lead of the component is coated with a simple flash of gold, there will not be enough gold in the solder for the danger limit to be reached. But visually, it cannot be seen. According to the precaution principle, the components with gold plated pins should, therefore, not be used.

The items to be observed in the category **"faults on connectors"** mainly concern card-edge connectors. We separate inspections of the male part (on the printed circuit) from those of the female part. The male part is more accessible, since the female part is located at the back of a cabinet of the instrumentation and control system. For the male part, the inspector should observe the following points:

- Presence of inorganic pollution (observation carried out in white light).
- Presence of organic pollution (observation carried out in ultra-violet light which reveals the presence of organic pollutants) [1-2].
- Signs of corrosion and/or oxidation.
- Presence of scratches on the tracks and estimation of their depth.
- Separation of the tracks by mechanical damage.
- Signs of arcing.
- Deformation of the indexing pin (if appropriate).

For the female part of the connector, the inspection involves assessing the following criteria, observed by endoscope:

- Observation of the vacuum spacing (directly visually by endoscope or using a calibrated camera).
- Signs of corrosion and/or oxidation.
- Presence of inorganic pollution (in white light).
- Presence of organic pollution (in ultra-violet light).
- Presence of scratches on the clips (note: this observation is very difficult owing to reflections from the external light source required).
- Damage to the plastic casing of the connector (base).

Each of these criteria forms an integral part of all inspections. If necessary, the inspection may be completed by an assessment of the compliance of the repairs with the frame of reference of IPC A 610 version D level 3. Even if it only covers the quality of assemblies, it is considered that a repair should not be worse than manufacture itself. One has also to refer to two other standards: IPC 7711 and IPC 7721). The relay may also result in specific, albeit limited inspections (in particular, visual inspection on a relay with a metal cover is meaningless).

Each of the criteria discussed above gives rise to an assessment with 4 levels of severity. These levels are "aesthetic", "caution", "alert" and "critical". They are defined as follows:

- "Aesthetic" means that a fault has been detected but that it has no impact on the long-term operation of the PCB examined (for example, the presence of dust in relatively small quantities or superficial scratching of the casing of a component not affected by oxidation).
- "Caution" means that a fault has been detected and if nothing is done, a failure is probable before the end of the board's life span (typically after more than 10 or 15 years).

- “Alert” means that a fault has been detected and it leads to a risk of failure or reduced reliability of the board within less than 10 years.
- "Critical" means that a fault has been detected and a failure is imminent or the failure is already present.

In theory, the four scores may be assigned to any of the observation criteria. In practice, certain faults are so serious that they cannot be “aesthetic” or even “caution”. For example, for card-edge connectors, the vacuum space between two clips of the same pair determines the contact force and, therefore, the contact resistance. When we detect visually that the gap is too wide, this means that the resistance value is already outside specifications (visual acuity is not sufficient to observe behavior at the limit of specifications). Accordingly, the inspector will have no other choice but to assign an “alert” or “critical” score it he detects such a fault. On the other hand, certain faults may never be “critical” such as, for example the presence of dust on the board.

Following the assessment of all the criteria described above, a final score is given to the PCB examined. It also has four levels possible:

- S (“satisfactory”): no criteria call into question the operation of the board under normal conditions for the next 20 years,
- M+ (“average +”): several faults may eventually reduce the reliability of the module and lead to failures. Repairs or backfitting are not essential,
- M- (“average -”): without corrective action, the electronic circuit board has a life expectancy of less than 10 years,
- NS (“unsatisfactory”): the board is far from the standard expected and a failure is imminent if no corrective action is taken. Such boards are generally withdrawn from service temporarily to await corrective action.

Finally and if necessary, the inspector makes recommendations concerning corrective action that could improve the board’s score. This may involve cleaning certain parts of the board, the preventive replacement of a component, the failure of which is considered to be imminent, the repair of tracks of the printed circuit, etc.

Examples of Observable Defects

Figures 2-2 through 2-9 illustrate some of the faults which may be observed during these visual inspections. Naturally, the list is by no means exhaustive.

Overall Appearance of the Printed Circuit

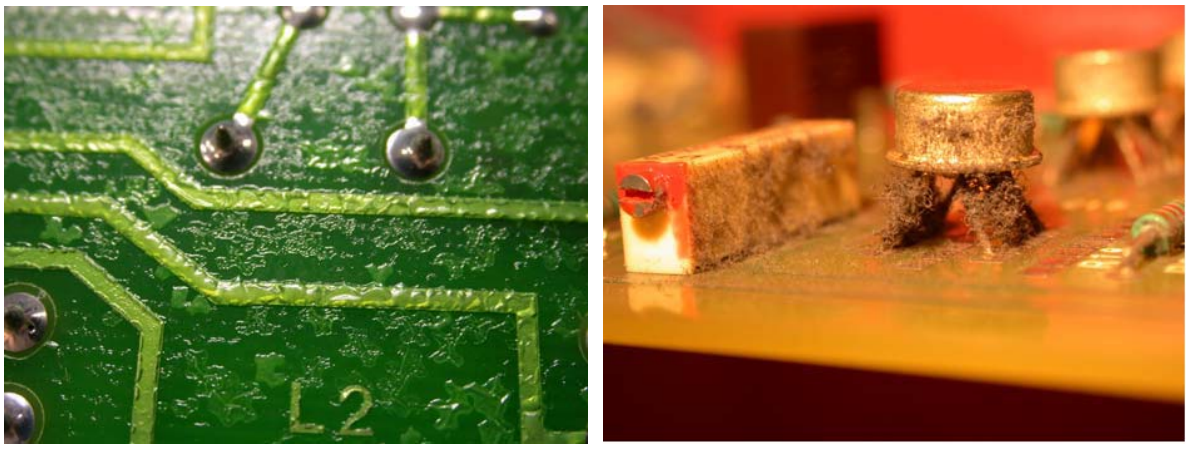

Figure 2-2
Faults in overall appearance of the PCB: (left) bubbles in the resistor (right) severe accumulation of dust likely to lead to short-circuits.

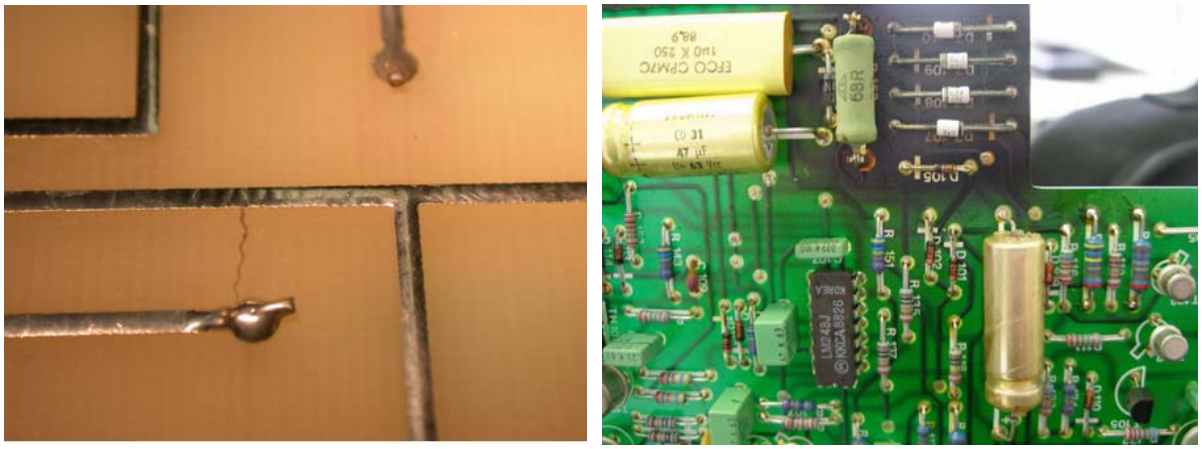

Figure 2-3
Faults in overall appearance of the PCB: (left) electromigration between two tracks of the PCB and (right) overheating of diodes (originally blue) leading to overheating of the PCB.

State of the Solders

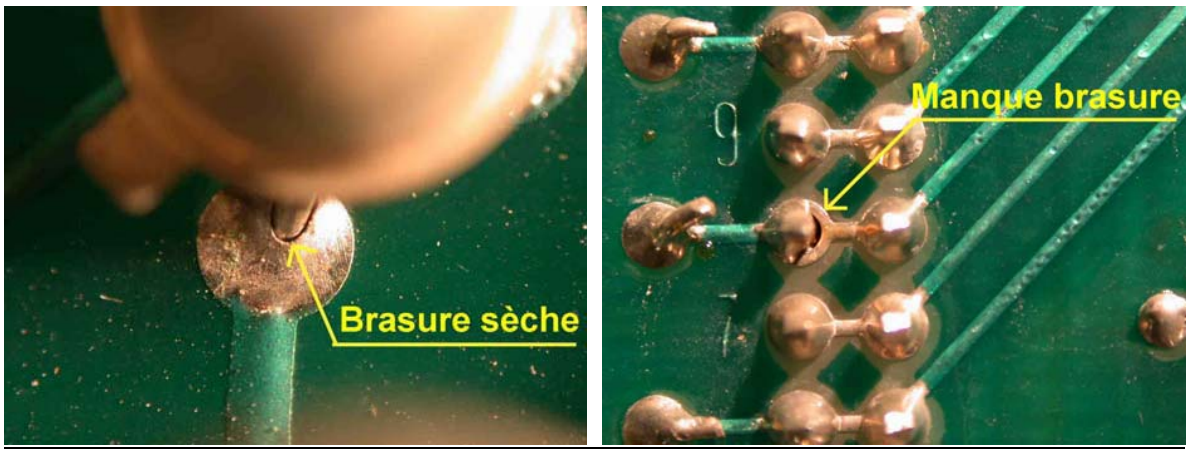

Figure 2-4
Faults on the solders (left) dry solder and (right) lack of solder.

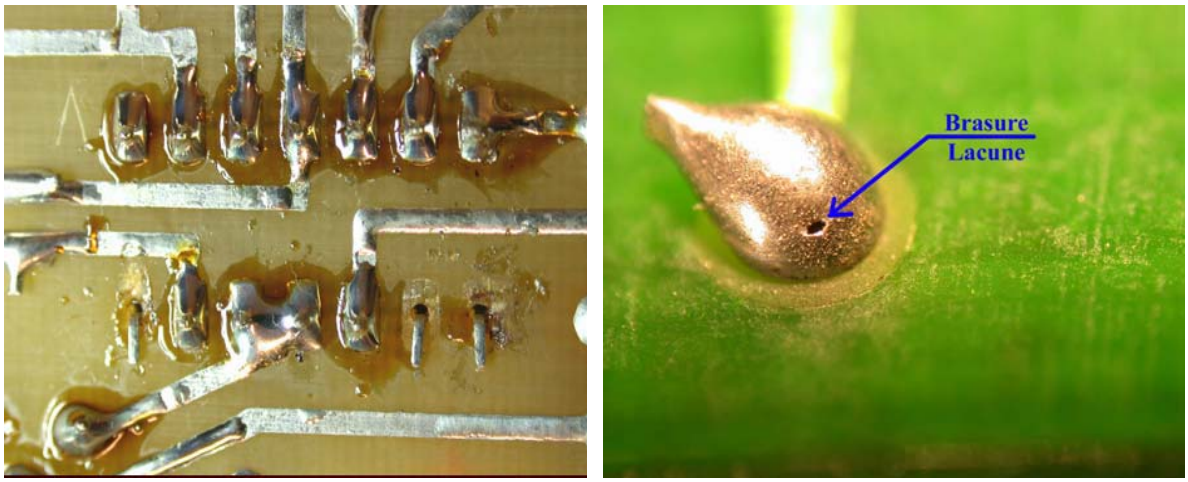

Figure 2-5
Faults on solders (left) residue of flux not cleaned and (right) lack of solder.

Faults Observed on Components

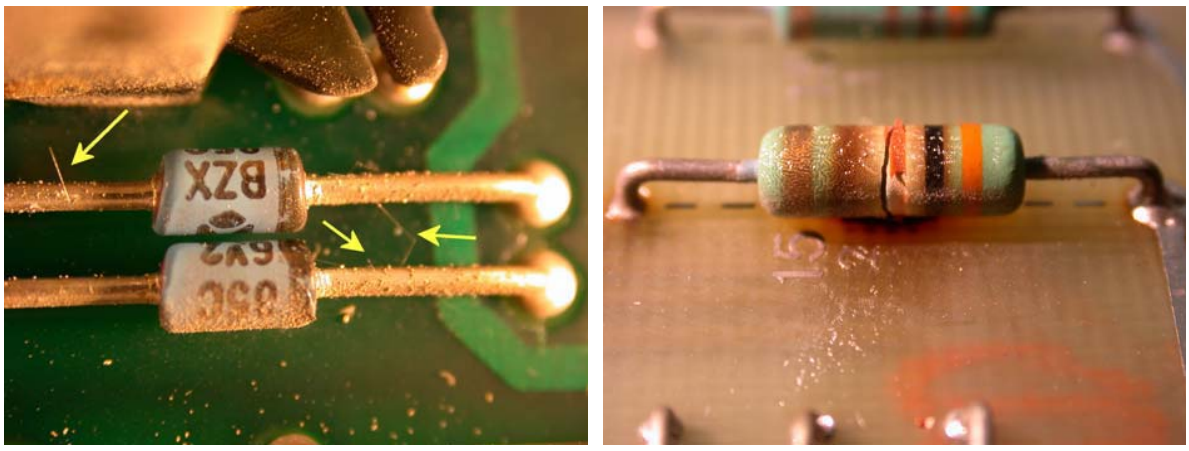

Figure 2-6
Examples of faults on components: (left) whiskers on BZX diodes and (right) crack of the package of a resistor.

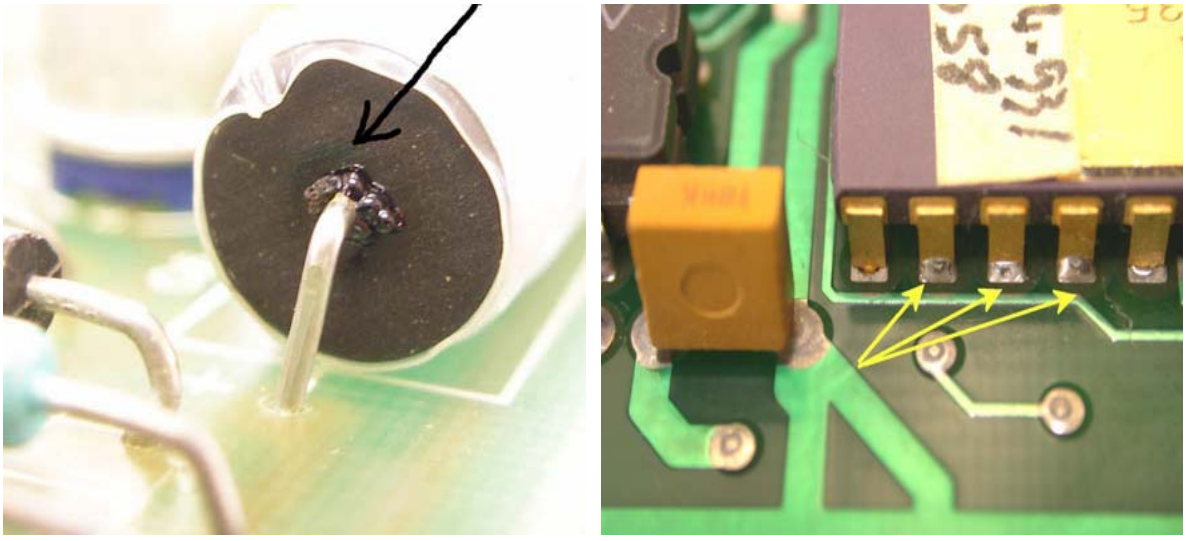

Figure 2-7
Examples of faults on components: (left): leak from an electrochemical capacitor and (right) solders on a component with a gold finish not previously stripped.

Faults Observed on Connectors

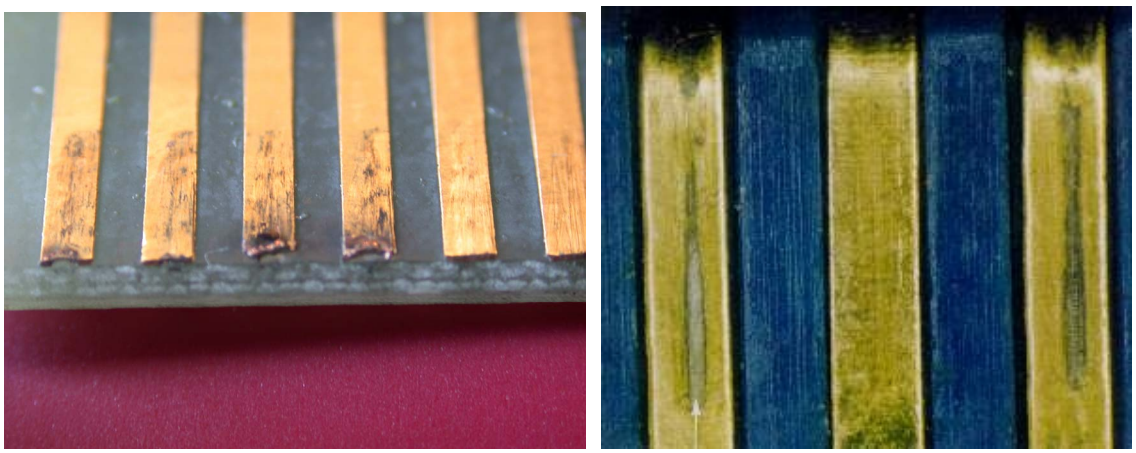

Figure 2-8
Examples of faults on connectors: (left) connector fouled and damaged and (right) deep scratch of approximately 5 µm that reveals and damages the coating of nickel under the superficial protective coating of gold, which could result in the oxidation of the contact.

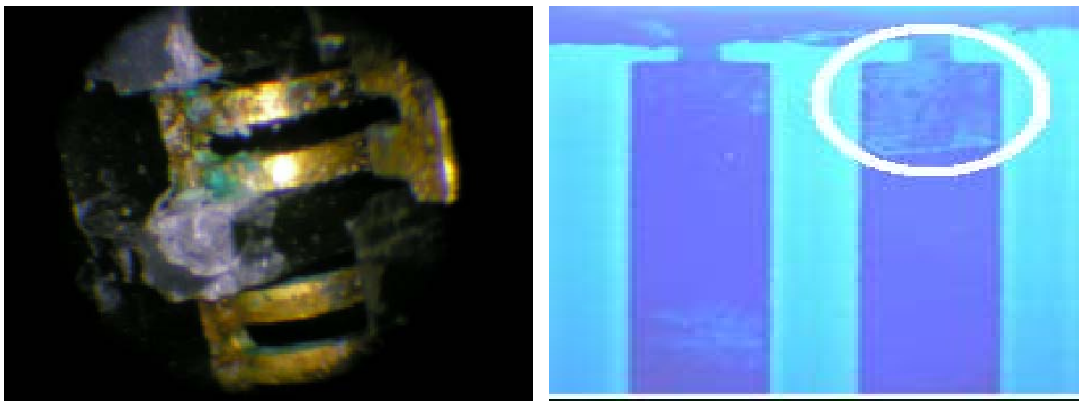

Figure 2-9
(left) female HE9 connector corroded and housing damaged (observed by endoscope) and (right) signs of organic pollution (observed in UV light) on a male HE9 connector.

EDF Inspection Approach

Inspections are carried out mainly by EDF R&D when preparing for the ten-yearly in-service inspections, as part of an approach known as “Monitoring of the aging of instrumentation and control systems” (OVCC in French) and currently applied to 900-MW units, on the one hand and those of 1300 MW, on the other. This approach is not yet in place for N4 units (1450 MW). The main instrumentation and control systems are inspected as follows, boards are chosen at random from each of the systems on various sites (typically at least 3 sites, one of which is a seaside site and one a river site, in order to exploit data from different environments). Therefore, on a

campaign of type OVCC (900 MW or 1300 MW), several hundred of boards are inspected individually. The data obtained are then collated for each system (for example “reactor protection”) which gives a good representation of the state of aging of printed circuit boards and forecast of their residual life span. These results provide a basis for making decisions as to whether or not to renovate an instrumentation and control system either partially or totally during ten-yearly in-service inspections.

It is clear that this approach, which is followed systematically every ten years, can only be limited in terms of scope (therefore to the OVCC in preparation for the third ten yearly in-service inspection of 1300-MW units, approximately 2000 boards have been examined. This number is certainly high but, when compared to the total number of printed circuit boards for all the 1300-MW facilities, it remains relatively modest). That is why it was decided to transfer visual inspection skills partially to the nuclear sites. EDF R&D has established training courses for site employees since 2010. The aim in the long term is to ensure that all boards handled for the purposes of maintenance are inspected. The results of inspections are subject to reports sent to EDF R&D which analyzes them, thus obtaining a much finer overall view of the state of aging than that determined following OVCC.

It must also be noted that this visual inspection technique is also used for trouble-shooting, spurious or transient faults. It does not only concern nuclear instrumentation and control systems, but is also very efficient for all instrumentation and control systems (typically for more conventional transmission, distribution or production installations (hydraulic, fossil fuel, etc.]), which enables inspectors to perform inspections often and, therefore, improve their expertise.

Limitations of the Technique

As mentioned throughout the previous sections, this method of assessing the state of aging of printed circuit boards is based only on visual inspections, occasionally assisted by optical magnification or special light sources. It is not yet intended to use sources such as X-rays, which would enable us to see through the packaging of the electronic components, for reasons of safety of instrumentation and control systems (this is currently under review). Accordingly, only external faults and aging (or internal faults with external consequences, such as severe overheating for example) can be detected. In particular, visual inspection reveals nothing about faults such as thick intermetallic compounds on bonding wires on chips, the local overheating of chips, the presence of damage due to electrostatic discharges (ESD) inside the component, etc. The same situation applies to multi-layer boards. In some cases there are no components in the internal layers, in other cases there are and these can not be observed visually. Lack of observability occurs with the recent technologies SiP (systems in package) and SoC (systems on chip). One can also find this problem with hybrid integrated circuits. For all such hidden faults, qualified as internal faults, other often destructive techniques have to be used and shall be described in Chapter 3.

Another limitation is due to the fact that the inspector does not have visual access to all the components with the right angle of view. He may be hampered by the presence of a solid component beside the one he wishes to examine. Therefore, lighting is not optimal and he is likely to miss certain faults (this is often the case for whiskers).

The third limitation to be mentioned is due to the density of metal components on the boards. While packages are often made of non-reflective plastic, this is not true of pads, solder and the component leads. These metal surfaces will generate reflections which will also hamper observations. Figure 2-10 gives an example of a highly integrated board with a high density of metal leads, which makes visual inspection difficult.

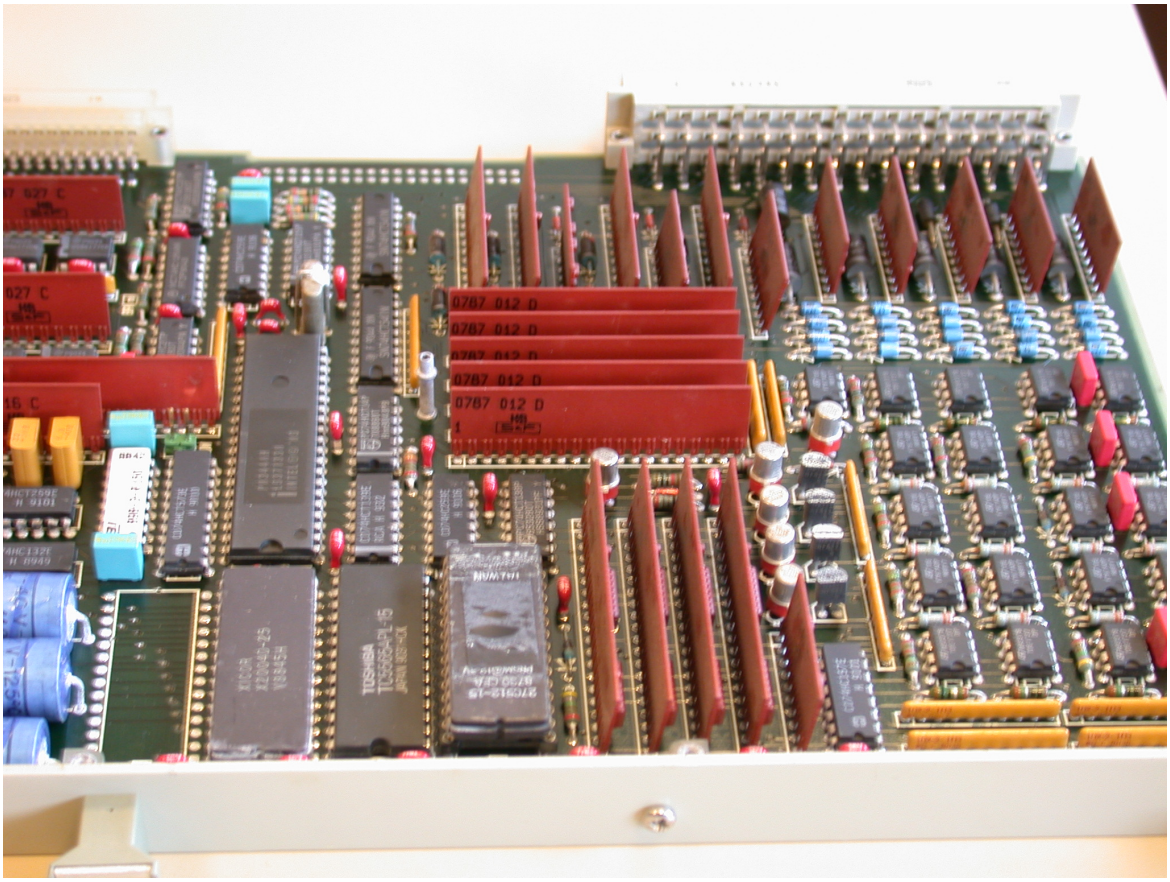

Figure 2-10
Example of an electronic circuit board for which visual inspection is difficult.

By combining these two points, it may be noted that the more a board is integrated, the more visual inspection is inaccurate.

Visual inspection with magnifiers is highly appropriate for older technologies (typically for systems put into service from the 1970s to the 1990s, which are the vast majority of the instrumentation and control systems in French nuclear power plants), because these systems have the following characteristics:

- There are no SMC (surface mounted components) or (in the worse case) BGA (Ball Grid Array) on the PCB.
- The density of components remains low.
- The number of ICs (integrated circuits) remains small.

- The PCB is not a multilayered board.

Newer technologies for systems that do not meet the above characteristics need more robust capabilities. These more robust capabilities are a current research issue at EDF R&D.

Summary

The visual inspection technique is the basic technique developed and used by EDF R&D for estimating the aging of electronic circuit boards and anticipating their residual life span. It is used very extensively but, while it gives relatively complete results that are easy to obtain, it is not sufficient for fine monitoring of aging and for defining the required preventive maintenance. That is why it is complemented by other more extensive inspections, which are described in the next chapter.

3
ADDITIONAL INSPECTION APPROACHES FOR PRINTED CIRCUIT BOARDS

Off-Line Analyses

Difficulties of On-Line Analyses

In order to be able to carry out the right maintenance operations at the right time without affecting the operation and reliability of boards by excessive handling (see Chapter 6), on-line diagnostics tools should be available for continuous analysis in real time. On-line analysis also enables us to anticipate failures and eliminates the need to carry out inspections requiring handling during the shutdown of the system concerned.

Nevertheless, it is very difficult to carry out such analyses. Indeed, the boards currently in service were not designed with on-line testing in mind. Adding a system for monitoring the board during operation will likely lead to disturbances of varying degrees on the board being monitored. If adding monitoring, it should be shown that in all possible cases, including incorrect operation of the monitoring system, operation of the electronic circuit board concerned is not affected. Therefore, if we wish to take an electrical measurement, we must ensure that there are no leak currents strong enough to alter the electrical levels of neighboring components (for example, change one bit in a memory, change of state of a diode, etc.). This is extremely time-consuming and explains why no good on-line measurements are currently available, with the exception of periodic testing. However, the purpose of periodic testing is to reveal any failures or even marked aging but in no case reveals signs of aging.

Furthermore, it is very difficult to use certain investigation techniques on site such as X-ray imaging methods, multipoint electrical testers, etc.

Therefore, it is simpler to look for off-line analysis solutions to overcome the problems raised here.

Capacitors

The passive components that pose the most problems from aging by far are capacitors of all types. This means not only electrochemical capacitors, but also ceramic and tantalum capacitors.

In all these cases, EDF R&D has developed a technique for the analysis of aging based on the impedance spectroscopy [3-5]. For this, the behavior of a capacitor was modeled by breaking it

down into an inductor, several resistors and capacitances in series or in parallel as shown on Figure 3.1. The model consists of three blocks, each of which corresponds to a given frequency range. At low frequency; cell No. 1 is used to characterize dielectric losses and insulation resistance at low frequency. It is important to note that resistance R1 depends on frequency. Cell No 2 reveals faults on the interfaces of the dielectrics at medium frequency. Cell No. 3 (high frequency) is a good indicator of the state of internal connections. For a more detailed model, we can include the dependency of resistance R4 on frequency.

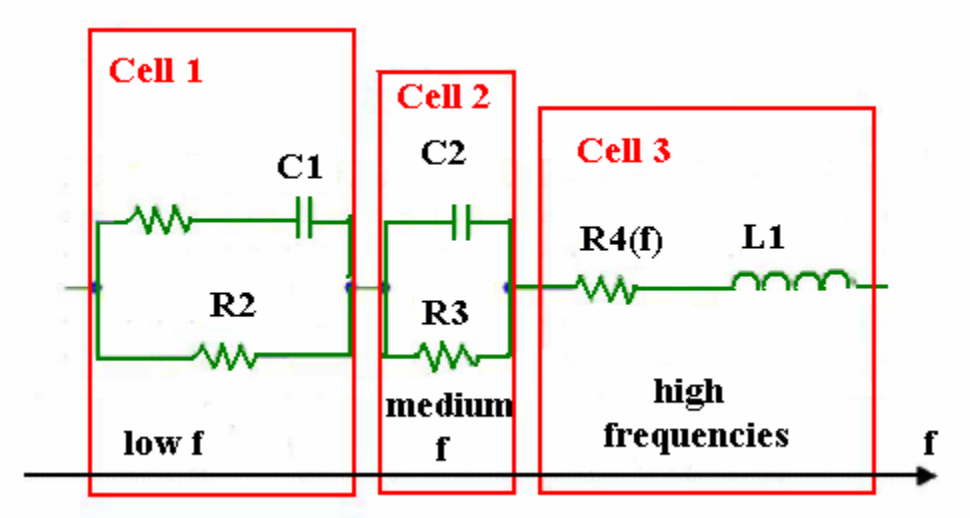

Figure 3-1
Modeling of the frequency behavior of a capacitor.

Once this model is established, measurement of aging involves the analysis of the spectral response of the capacitor in a range from 40 Hz to 5 MHz. After the spectrum has been recorded, we must identify the values of each of the parameters of the model by simulation. Specific points (such as the value of resonance frequency) are used to determine the parameters of interest, as shown in [3], quite quickly.

In many cases, the values of the parameters of the equivalent diagram are used to determine the state of aging of capacitors, particularly for electrochemical capacitors and tantalum capacitors, for which the relatively simple criteria may be used:

- For electrochemical (aluminum) capacitors, we should monitor, in particular, changes to parameter R4 and parameter C1, which have proven to be early aging indicators. Aging is also indicated well by the measurement of the frequency of equivalent series capacitance, as shown on Figure 3-2. With aging, resonance is reduced and the appearance of the frequency response curve of equivalent series capacitance is greatly altered.

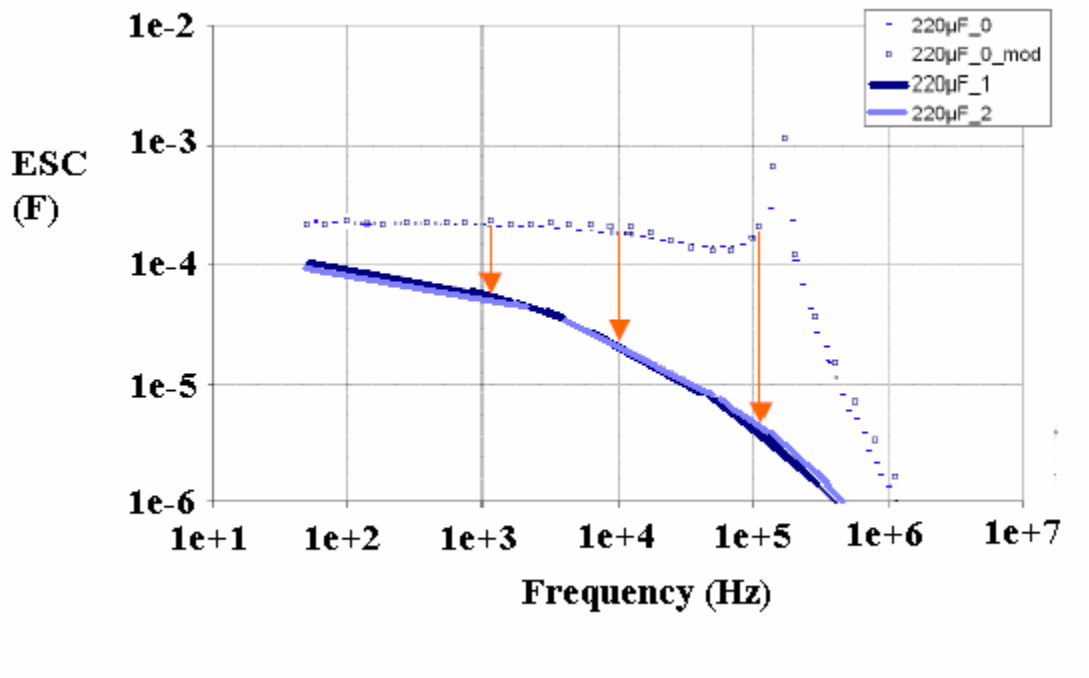

Figure 3-2
Frequency response for frequencies between 50 Hz and 1 MHz of a non-defective electrochemical capacitor of 220 µF (top curve with its model once the parameters of the model are identified) and two defective capacitors of the same capacitance. The arrows represent the changes to the curve with aging.

- For tantalum capacitors, the studies show that there is no significant variation in parameters C1 and R4. On the other hand, the study of cell No. 2 (intermediate frequencies), characterizing the interface oxide reveals a change to parameters C2 and R3.

It is important to note that these measurements are non-destructive and that the study of the frequency response of the other passive components (resistors and coils) also gives good results, which are less easy to exploit than those for the capacitors, but which enable us to detect the first signs of aging.

These measurements should be carried out on a regular basis but may be a year or more apart. Any changes to the mechanisms are quite slow.

Thyristors

It is also possible to anticipate the aging of certain power components, such as thyristors [6], quite simply. According to the literature [6], thermo-mechanical aging due to power cycles is the main aging mechanism. It results in damage to the blocking characteristics. This is not the case for thyristors studied by EDF R&D (thyristors TS1235, TK1120 and TK12 [switching thyristors]). Indeed, no correlation has been found between the number of power cycles and any electrical drift observed. Accordingly, the only electrical characteristic of the thyristors which varies after 20 years is the trigger current threshold. Indeed, given their design, such thyristors

are not subject to thermo-mechanical aging. Figure 3-3 shows a cross sectional view of a thyristor and the operating diagram.

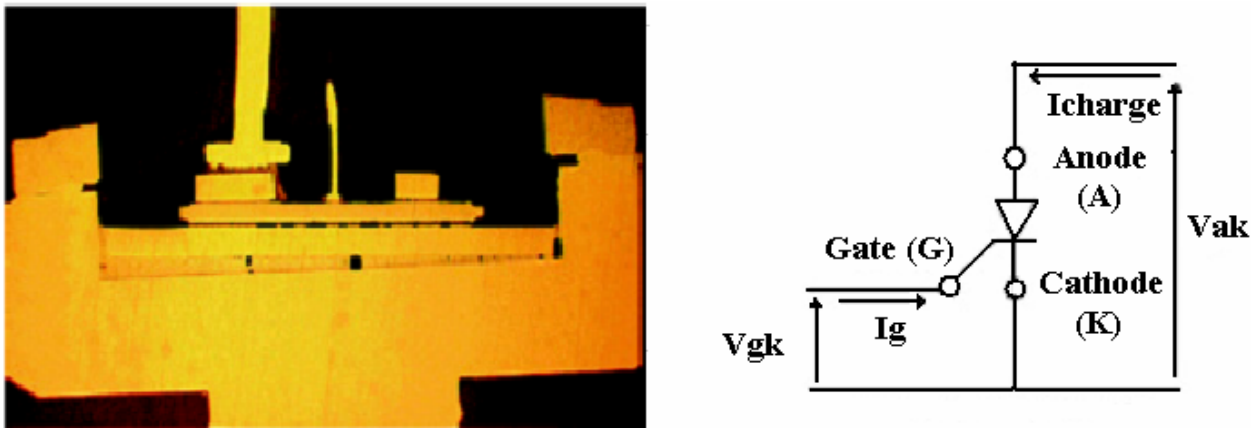

Figure 3-3
(left) cross-sectional view of a thyristor and (right) electrical circuit diagram.

To determine the aging of such thyristors, we should; therefore, measure the trigger current. Studies have shown that the variation of trigger current is generally accompanied by significant drift of the holding current. Accordingly, the thyristors go out after suppression of the command. Similarly, high leak currents appear. Several causes may explain the variation in the trigger current during aging. The two main causes are:

- A manufacturing fault, such as the misalignment of the cathode-trigger assembly.
- Aging of silicon, which may be natural.

Some of the other possible causes are:

- Misalignment of the cathode-trigger assembly.
- Ionic contamination of the die.
- Natural aging of silicon.
- Crack in the die.
- Damaged contacts at the die level.
- Corrosion of the contacts (at the die or at the component level).

A measuring instrument has been developed for the measurement of parameters I_g and V_{gk} at the same time. The principle of measurement is that the grid current is increased gradually until the thyristor switches. This illuminates a light emitting diode (see diagram on Figure 3-4). The trigger current is then measured and compared to the value given on the datasheet.

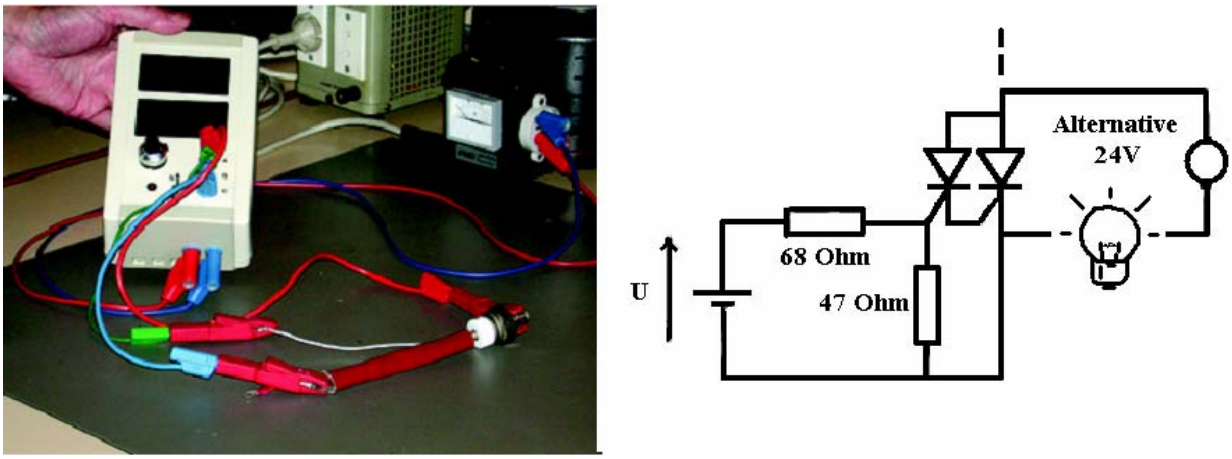

Figure 3-4
(left) Measuring instrument developed for measuring the aging of thyristors, and (right) circuit diagram with a LED which is used to indicate the switching of the thyristor.

Optoelectronic Couplers

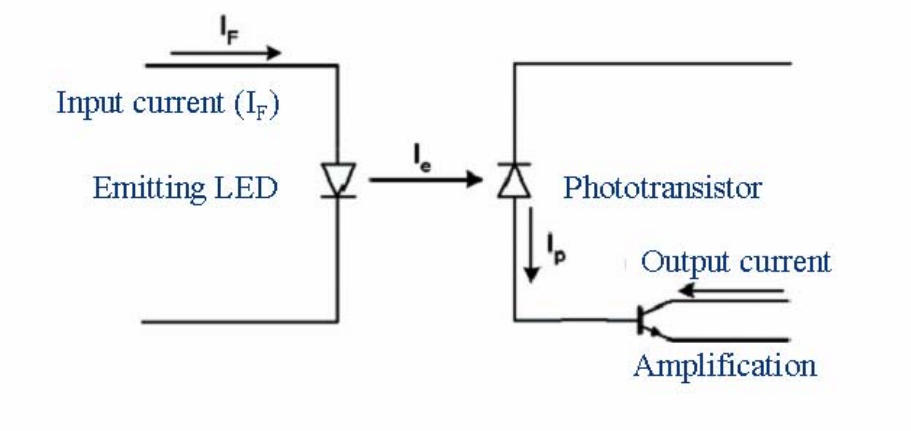

Figure 3-5
Circuit diagram for an optoelectronic coupler.

Optoelectronic couplers are also components where, the aging is quite easy to detect early. The circuit diagram for an optoelectronic coupler is shown in Figure 3-5. The main causes of aging of optoelectronic couplers are as follows:

- A reduction in the efficiency of the light emitting diode which results in fewer photons passing between the light emitting diode and the phototransistor (resulting in a drop in output current).
- Opacification of the interface between the two diodes of the optoelectronic coupler, thereby reducing the number of photons reaching the phototransistor (resulting in a drop in output current).

- A reduction in the efficiency of the phototransistor and amplification. Here the number of photons reaching the phototransistor is correct but amplification is not sufficient, which reduces the output current.

In each of these cases, it would appear that the common parameter indicating signs of aging is the ratio between output current and input current. The measurement is made very simply by measuring an imposed input current and the resulting output current, at the same time. The instrumentation may be very simple. The tool used by EDF is shown in Figure 3-6 and is just connected to the optoelectronic coupler.

Figure 3-6
Example of a tool used to measure the ratio between output current and input current.

Other Power Components

As a general rule, aging indicators may be found on power components. We refer here to diodes and power transistors, thyristors, triacs and IGBT (main low voltage switch).

These components age in particular due to the fatigue of internal solders (typically the joints between the chip and the heat sink). Such fatigue is due to variations in temperature during power cycles and leads to the cracking in these joints. This mechanism will lead to an increase in the thermal resistance of the assembly and takes the form of an increase in the temperature of the casing. This parameter is determined by the use of an infrared thermal camera. The measurement may be made on-line.

On the other hand, if we wish to determine the state of aging (particularly problems due to the migration of ionic contaminants in the casing, resulting in an increase in leak currents and a drop in the maximum blocking voltage), this parameter should be measured by an electrical test. Now this measurement can only be made off-line. Even if it is very simple in terms of design, the component should be insulated to avoid any spurious measurements.

Complex Active Component

Until now only passive components and simple active components (components which sometimes incorrectly classified as passive components) have been discussed. The case of complex active components is more interesting since they perform more functions and generally play a key role in the operation of the board. However, it is very difficult to test (even off-line) active components on site. Indeed, the testers for them are particularly large and cannot be moved; such as multi-point testers for example. Only analysis in the laboratory enables the behavioral drift (and aging) of these components to be studied.

Destructive Testing of Components

Principle

To go further in the detection of aging and understanding of the causes of failures of components, the destructive testing of a component is the best technique currently available [7]. This form of testing consists of examining the active parts of components. It starts with the removal of the electronic component from its casing to examine its internal structure. Analysis is then much more detailed than from a simple visual inspection. This analysis approach continues with the use of various analysis techniques such as:

- X-ray examination: this non-intrusive, non-destructive technique is intended to see through plastic or metal casings and diagnose a certain number of obvious mechanical faults. We shall seek in particular to identify problems of loss of electrical or mechanical continuity (failure of the power supply wires of a coil in a relay, bonding wires not connected on a chip, etc.). This will guide our choice of complementary techniques for the rest of the analysis. In general, for relays and active components, X-ray examination is always the first step in the analysis of a failure.
- Observation in ultra-violet radiation: used mainly for contacts (relays, connectors, etc.), the ultraviolet light is used to reveal organic pollutants which act as a third body and affect the quality of the contact.
- Observation by scanning electron microscope (SEM): the SEM is the ideal tool for the analysis of failures. It provides, in particular, for the observation of small structures on chips and for the exploitation of micro sections. The surface observed is excited by a high energy beam of electrons and we are interested in back scattered or secondary electrons emitted by the surface being analyzed.
- Elementary analysis of components by energy dispersive X-ray spectroscopy (EDX): an EDX probe is associated with an SEM and is used to determine the nature of the elements present in its beam of electrons. The measurement is generally semi-quantitative. It is very useful for reverse engineering studies or for revealing the presence of unexpected elements (for example, it may be shown that the lead of certain electronic components is made of an iron-nickel alloy which will eventually corrode).
- Micro section: this is a cross section taken along a given axis in a component. The cross section (or micro section) is used, combined with an SEM, to make observations within the material itself. The disadvantage lies in the fact that the number of cross sections per

component is necessarily limited and it is; therefore, useful to make first level diagnoses beforehand (by X-ray for example) to locate the fault as accurately as possible.

- Fourier transform infrared spectroscopy (FTIR): this technique is complementary to EDX and is used to discover types of atomic bonds. The principle is as follows. A sample is exposed to infrared radiation and the radiation absorbed by the sample is measured according to wave length. Each wave length corresponds to a specific chemical bond which gives the type of material concerned by cross-checking. This technique is particularly used for the analysis of packaging by reverse engineering (in order to determine the materials used and predict their aging behavior) or by seeking to modify their properties in relation to their initial properties (in particular, for polymer packaging materials, excess heat may modify the conformation of molecules).
- Infra-red thermography: with this technique, we use the infrared radiation emitted by a component (in this case the technique is non-destructive) or by the chip of an integrated circuit under normal operating conditions with no additional stress. The aim is to locate hot spots or spots that are hotter than expected. It is then possible to locate a failure quite accurately.
- Acoustic tomography: this can be carried out before opening the casing. This method of analysis is based on the propagation of sound. Generally, the component or the PCB is immersed in a shallow depth of water and ultrasound is applied to the surface of the sample. We then measure the acoustic wave reflected by the different interfaces or that transmitted through the sample. After appropriate processing of the signal, it is possible to detect problems of adhesion between two internal layers (in the middle of a multilayer PCB for example), delamination, etc.
- Emission microscopy (EMMI): this is a non-intrusive optical analysis technique used on the chip of a component in order to detect certain specific faults, such as the consequences of ESD (electrostatic discharges – see below), the susceptibility of a circuit to the phenomenon of hot electrons, certain leak currents, latch-up or problems of floating gates. The aim is to view faults using their signature in the visible or near infrared band when the component is in operation. It provides for very accrual physical location of the fault.
- OBIRCH (Optical Beam Induced Resistance CHange): OBIRCH [8] is the most commonly used laser thermal stimulation technique. The laser stimulation will lead to thermal changes inside the chip and reveal the differences in thermal behavior between a sound area and a defective area in the same chip. This difference will mainly be visible on the resistance of the zone heated. OBIRCH is mainly used to reveal problems due to electromigration. There are other similar techniques, such as XIVA (eXternal Induced Voltage Alteration) and TIVA (Thermally Induced Voltage Alteration).
- Pull test and shear test on bondings: after opening the casing, it is possible to carry out mechanical pull and shear tests on the bonding wires on chips to make sure that the wire is secure and test for the presence of excessive thickness of intermetallic compounds (IMC) on the interface between the pad and the bonding. We also can detect other problems, such as brittleness of excessively fine bonding wire.
- Measurement of the integrity of passivation: the aim here is to measure the dielectric properties and homogeneity of the various passivating layers.

There are many techniques that could be used and the list above, which is far from being exhaustive, gives those most often used by EDF R&D. It should be noted that most of these techniques are only used for active components. For passive components, such advanced techniques are only very rarely used, since failure modes are much simpler and a simple micro section, together with SEM examination, if necessary, is enough to find the cause of the failure. Furthermore, the causes of failures of passive components are very limited. Accordingly, they are not checked systematically, allowing greater concentration of efforts on active components.

Extrapolation to the Anticipation of Aging

The destructive testing of components is a technique so powerful that it is not limited to the analysis of failures, it also enables us to detect of the signs of aging well before the appearance of a failure. It is possible to perform such tests on components sampled at random in operation to assess their aging. These methods are particularly useful for estimating the aging of solders.

Indeed, for solders made of $Sn_{63}Pb_{37}$ (the vast majority in French nuclear power plants), observation of the microstructure is the only technique capable of determining the state of aging of the solder. The term microstructure refers to the shape, size and overlapping of the different metallurgical phases in the solder. This is visible on Figure 3-7. The image on the left shows the micro section obtained from a slightly aged solder. We observe a relatively disordered structure. On the other hand, the image on the right shows the micro section of a solder after aging (30 years in operation). We observe that the phases of lead are ordered and that a dendritic growth of this phase has occurred. In general, the longer a dendrite and the more arms it has, the more the solder has aged. In the long term, the phase coalescence will weaken the solder so that it will no longer serve its mechanical purpose. Furthermore, the micro section is used to measure the thickness of the intermetallic compound (IMC) between the PCB and the solder and between the component and the solder. IMC that is too thick will lead to loss of adhesion of the solder on the PCB or component. Furthermore, excessive thickness of an IMC will prevent the component from being repaired back into good condition, should it fail. Moreover, in the literature the change in the thickness of IMC is modeled by various empirical formulae, such as Hwang's formula [9] or Engelmaier's model [10], which have been updated since the publication of the RoHS directive, or their derivatives and less complete versions.

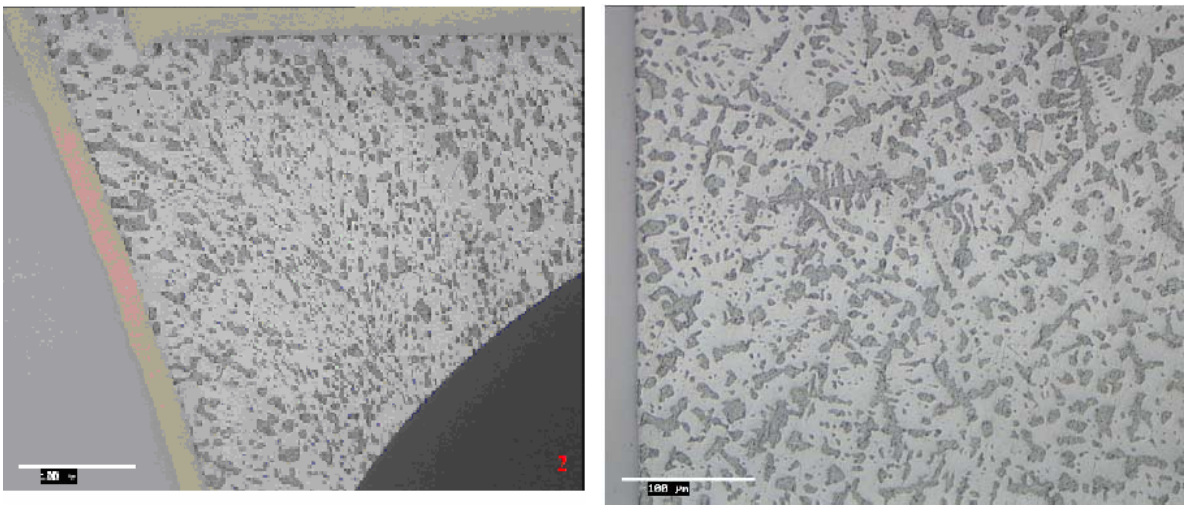

Figure 3-7
Aging of the microstructure of solders (left): solder less than 5 years old: (right): solder after aging for 35 years [11].

Another interesting aspect is that when the role of such solders is known (namely the service life of the board and the temperatures it is exposed to during its life), it is possible to trace the residual life span of the solder on the basis of these empirical models. This enables us to anticipate future failures.

Coverage Ratio and Rate of False Failures

Destructive testing is also a good way of determining the coverage ratio of a tester and the rate of false failures or RAS (Nothing to Report). For information, a RAS is a component (or electronic circuit board) deemed to be defective but for which no failure was found during electrical tests carried out once the circuit board was removed from its slot. There may be several possible reasons. First, the board is not actually defective and was sent for repair by mistake. Second, the board may be defective but the tester used during the repair and/or analysis of the failure was not comprehensive enough to confirm the failure (in this case, we talk of inadequate test coverage). If destructive testing reveals a physical cause of the failure, it is obvious that the testing procedure should be revised to improve the coverage of the testing. On the other hand, if no failure signature is found, it is not possible to know whether the component was actually functional before the analysis or if, on the contrary, the failure is real but the analysis was not detailed enough to reveal signs of failure.

It should be noted that this approach may quickly become very time-consuming and costly. Let us take the case of a component reported as defective by the personnel of the power plant but found not to be defective during the electrical test. Generally, the procedure followed at EDF means that for as long as the board has not had its third RAS, it is re-qualified if necessary and put back into service. Following the third RAS, it is scrapped and sent to EDF R&D, which may decide to carry out a destructive test post-mortem. In this case, it is not possible to direct the failure analysis in advance since we have no idea of its cause as the fault has not been confirmed. We must, therefore, resort to very detailed analysis using a large number of analysis techniques (which are not always compatible: for example, when we take a micro section it is very difficult to take several cross sectional planes on the same chip of a component). Such an analysis of an active component typically costs more than 5,000 per component (and may, in certain extreme cases exceed 20,000 per component, particularly when detailed analyses of the chip are concerned), not counting the time required to carry it out. That is why EDF R&D only occasionally conducts destructive tests on the boards scrapped owing to RAS (less than one case in ten). It is preferable to try to assess the coverage ratio of a tester and test RAS boards on other additional test benches to check whether these test benches confirm a failure not detected by the first test bench.

Some Examples

As mentioned above, destructive testing is used to reveal internal failures. This section describes a certain number of detectable failures taken from failure analyses carried out by EDF R&D.

- Wiring fault between the chip and the leads of an SN74LS244 type component in a DIP20 type casing. The images taken with the SEM and shown in Figure 3-8 show a direct contact between the wire of pin 2A4 and the chip, leading to a leak current causing the leak observed in the electrical test on the component. Furthermore, there is a virtual contact between two wires (left hand side of the image); nevertheless, zooming in shows that while this position is not normal, there is no contact.

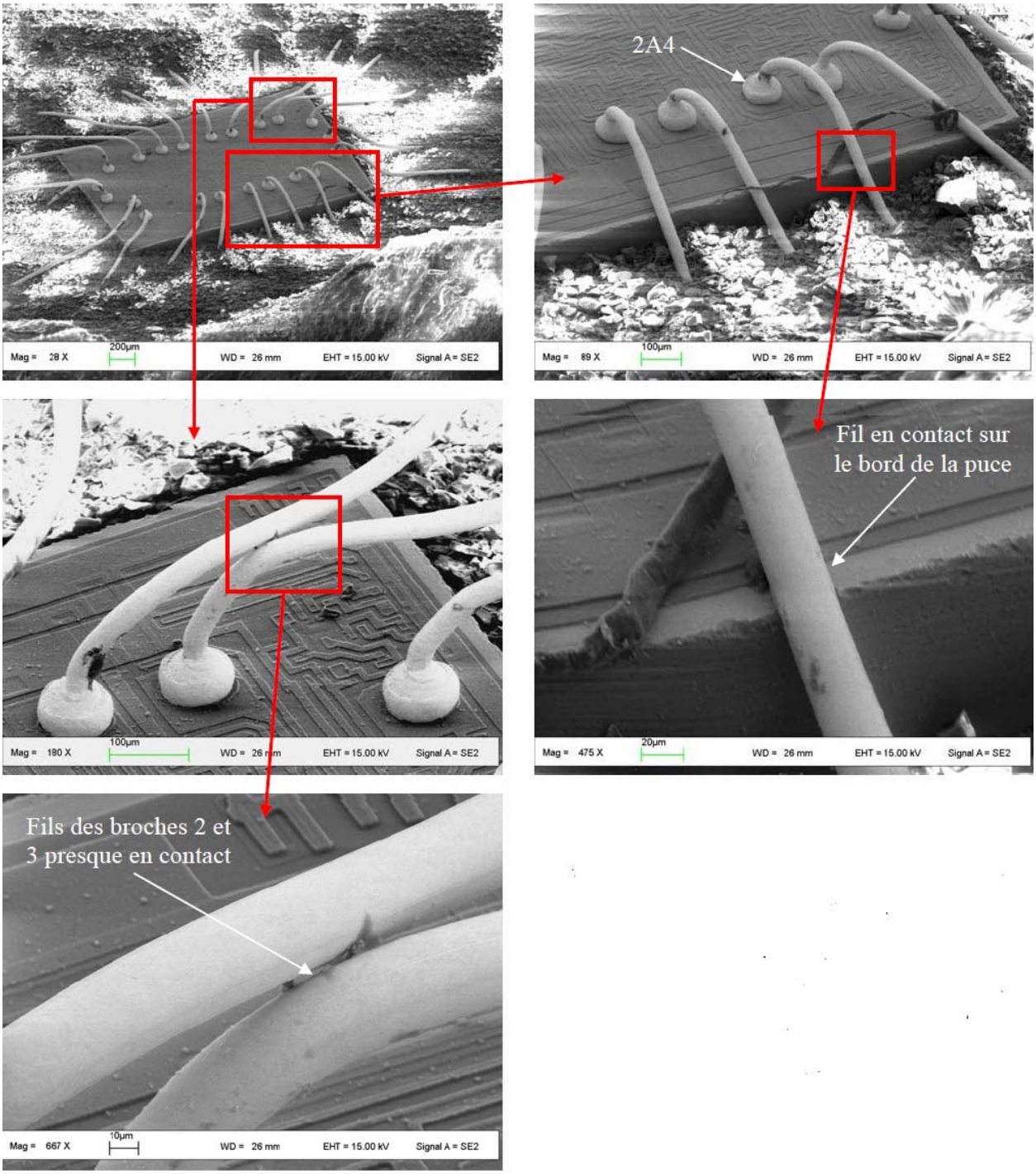

Figure 3-8
SEM images of the chip of a Texas Instrument SN74LS244N.

- Electromigration on the chip of a DM74LS279N (RS flip-flop) in a DIP16 casing manufactured by National Instrument. The electrical test revealed a VOL parameter with an abnormal value on one of the four outputs of the flip-flop. A lack of metal on the suspect circuit due to a phenomenon of electromigration, shown after opening on the SEM image (see Figure 3-9), followed by damage to tracks, caused the failure observed.

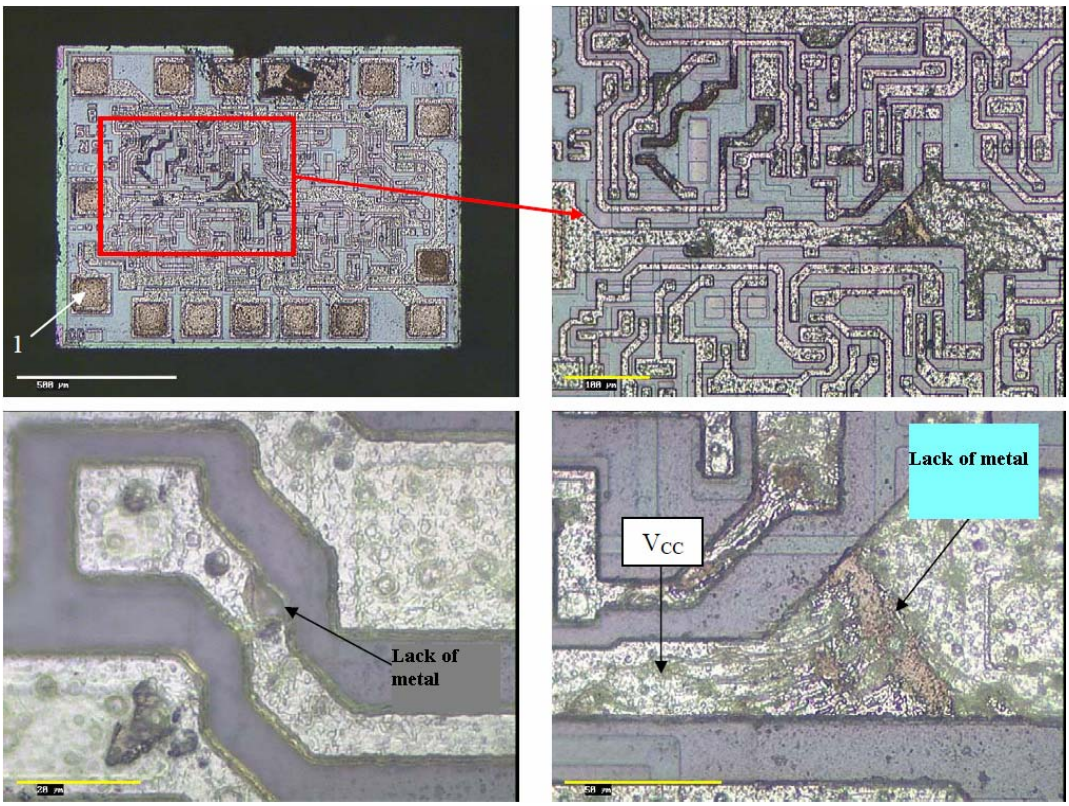

Figure 3-9
Lack of metal, effects of electromigration on the chip of a RS flip-flop.

- Migration of aluminum (electromigration) on a track connected to the VSS input of a Mostek MK4118P-2 (SRAM memory), leading to cracking of the passivation and extrusion of aluminum on the surface of the chip and failure (see Figure 3-10).

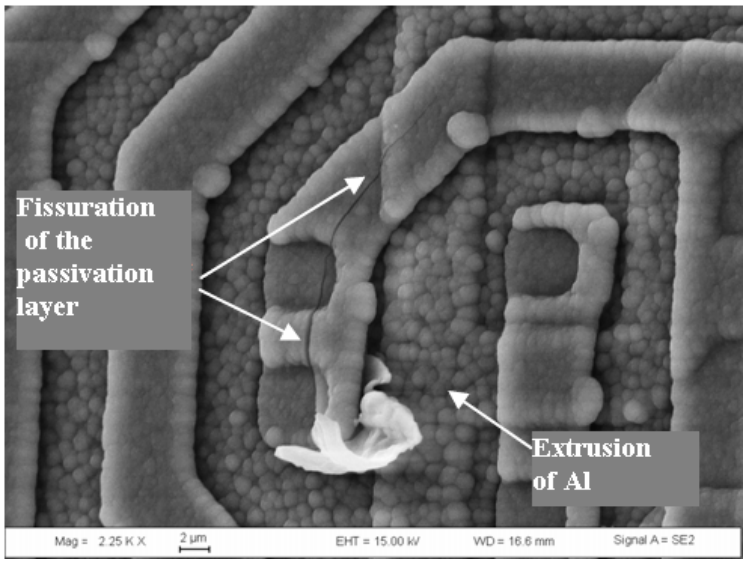

Figure 3-10
Presence of cracking and extrusion of aluminum on the chip of a SRAM memory.

- Oxidation and presence of impurities on a BZX85C diode owing to loss of sealing of the casing. A defective BZX85C diode was immersed in a bath of a fluorescent liquid under pressure. Figure 3-11 clearly shows in ultraviolet light, that the liquid has penetrated the diode as far as the chip. A micro section of the chip then confirmed the presence of impurities and oxidation, explaining the failure observed.

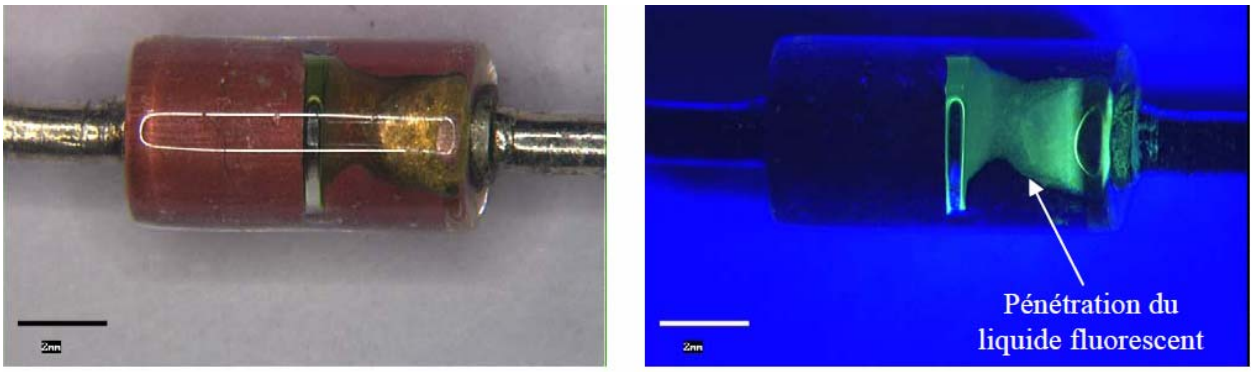

Figure 3-11
(left) BZX85C diode in white light (right) and in ultraviolet light after being placed in a fluorescent liquid under pressure.

- Presence of resistive filaments in the chip of a 2N2222 transistor probably due to a partial electrostatic discharge (see Figure 3-12). These filaments were observed by emission microscopy (EMMI).

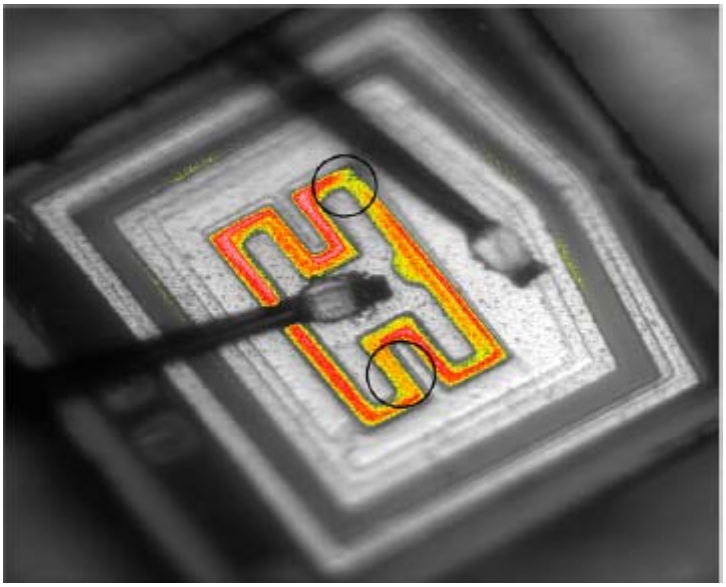

Figure 3-12
EMMI image of the chip of an almost defective 2N2222 transistor.

Actions to be Taken After a Failure Analysis

Once the failure analysis has been carried out, it is important to document it in a data base including as much information as possible. Ideally, it should include the following data at least:

- Type of component.
- Date-code.
- Manufacturing plant.
- Cause of failure.
- Site concerned.

Generally, the first three items are mentioned, with varying degrees of clarity, on the packaging of the component analyzed. EDF R&D has over the years collated a data base with some 2000 failures (for the entire stock of electronic components with EDF, not only from nuclear power plants). Therefore, it is now possible to take the failure analysis approach to the limit by making correlations between the various parameters. Now it is relatively easy to detect:

- Generic failures (same type of component, observed on several sites and for components from various manufacturers).
- Problems in manufacturing (series of poor quality, etc.), these failures concern a specific date-code or given plant.
- Cause specific to the environment or maintenance policy of a site (if failures of the same type are observed on a single site).

Nuclear facilities are now capable of taking appropriate measures (preventive replacement of the components installed, modification of MRO practices, etc.).

Recommendations for the Use of Failure Analysis

On the basis of the previous discussion, it is clear that EDF R&D is relying heavily on the destructive testing of components, which forms part of the following approach:

- Systematic destructive testing of defective active components in order to determine the cause of the failure and, of considerable importance, whether this failure is generic or not. For information, in 2010 EDF R&D has analyzed more than 300 active components considered to be defective by systematic analysis.
- Research into aging of components, the properties that drift but are still within their specifications. In this case, the analysis is not systematic. It is only carried out when the drift observed concerns sensitive equipment or when it appears to be generic. Such an approach was used; for example, for 2N2222 transistors [12-13].
- Regular monitoring of the aging of solders. Given the slow rate of change to the microstructure of solders, it is not necessary to carry out these analyses annually. Overall monitoring of representative boards, carried out once every five years for example, is more than enough. For information, EDF R&D carried out analyses of this type in 2009 and has not scheduled to do them again, given the good state of aging observed.
- Determination of the rate of NTD (Nothing To Declare) and the coverage of the testers used.
- Setting up a data base of the failures or aging components observed.

Monitoring Reports from PCB Repairers

As shown in the previous sections, failure analysis is a powerful tool for anticipating failures. Nevertheless, it requires an enormous amount of time and it is not always easy to do systematic analyses of the components found to be defective. Another useful indicator is provided by the PCB repairers themselves, who count the number of components actually replaced every year. This provides very reliable trends for the aging of instrumentation and control systems and it also detects significant increases in the number of failures for a given function or type of board.

Ideally, the repairers' statistics on the causes of failure should be compared with those from EDF R&D. At present, this comparison is planned but has not yet been made.

Summary

In addition to purely visual inspections, various additional methods for assessing the aging of printed circuit boards have been described here. On one hand, specific testers may be developed in order to analyze the main aging mechanisms suspected. This is true for passive components (capacitors in particular), optoelectronic couplers, thyristors and, more generally, power components.

The best method for determining the state of aging or finding the cause of a failure is still destructive testing. It should be carried out systematically on all defective components but also on an individual basis on aging components to assess their precise state of aging and predict their residual life span. Given the destructive nature of these analyses, it is obvious that the number of components just aging tested this way should be limited.

To stipulate the types and volume of components to be analyzed, we should also study PCB repairers' reports, in addition to results from destructive testing.

Therefore, by combining visual inspection techniques with the good practices described in this chapter, it is possible to obtain a reliable view of the state of aging of installations, not taking system level into consideration but electronic components themselves.

4
TECHNOLOGY WATCH OF OPERATING EXPERIENCE IN OTHER INDUSTRIES

Until now, only studies that could be carried out internally have been mentioned. As we have seen, they are very effective for determining the state of aging and making recommendations of all kinds to limit such aging. They also are effective in improving the maintenance of operational conditions. Nevertheless, these studies should be complemented by a view of what is happing outside the nuclear field. This can be done through advanced technology watches with three main objectives. The first objective is to gather data on the aging mechanisms of electronic components currently used in plants. The second objective is to gather information to improve our knowledge of components not yet installed in plants, but which could be used in the event of renovation or backfitting for obsolescence (or which could be used for the construction of new power plants). Finally, the third objective is to keep ourselves informed of the latest failure analysis techniques for the on-going improvement of the anticipation of aging and awareness of every more tenuous warning signs of failures.

To be optimal, the technology watch is carried out in two ways in parallel:

- Monitoring of the state of the art of aging and methods of analysis by reading publications in the field (typically, magazines such as Microelectronic Reliability) and following conferences, such as ESREF (European Symposium on Reliability of Electron devices and Failure physics and analysis) or ISTFA (International Symposium for Testing and Failure Analysis), the proceedings of which are often accessible.
- Taking part in networks of experts made up of companies, other industrial sectors (defense, transportation, aerospace, petrochemical, etc.), whose lifespan, environmental and/or reliability problems are similar to those encountered in nuclear power plants. These networks of experts provide for exchanges on good maintenance practices, analysis techniques, etc. and for an early warning network, within which information on components found to be defective passes.

5
CRITICALITY OF COMPONENTS AND PREVENTIVE MAINTENANCE

Components Sensitive to Aging

Following the analyses discussed in the above chapters, it is possible to draw up a list of components sensitive to aging and a list of those for which it is considered that their design life shall not be reached. To draw up this list, we must concentrate on components found to be defective by repairers. Once the causes of failure have been revealed, it is time to check non-defective components for signs of aging to determine the generic nature of the mechanisms observed.

This approach has revealed certain families of components or, in certain cases, specific components with specific dates and places of manufacture. The following in particular should be addressed:

- Optoelectronic couplers and, in particular MCT210 components. It must also be pointed out that in all applications of electronics, including fields other than nuclear, optoelectronic couplers are often said to be the weak link in the life span of printed circuit boards. For more details, please refer to Chapter 3.
- Electrochemical capacitors (see Chapter 3).
- Batteries which should be replaced on a regular basis, in accordance with the expiration date given.
- Logic components, the pins of which are made of materials sensitive to corrosion or oxidation, particularly those with solid iron-nickel alloy leads. This particularly concerns Texas Instruments components manufactured at the beginning of the 1980s in factories in Portugal, England and Malaysia. Components where the leads are made of an iron-nickel alloy are generally coated with silver. In time, this silver coating is porous to corrosive agents and degrades all the more quickly as corrosion enters it (corroded iron-nickel alloys will tend to swell, thereby cracking the silver coating which will become even more porous). Such materials are inappropriate even in moderately difficult environments, such as those of a nuclear installation, for operation over several decades. The evolution on such components is easy to follow in the sequence shown in Figure 5-1. At first, corrosion does not affect the operation of the component, but this is no longer the case in the final stages.

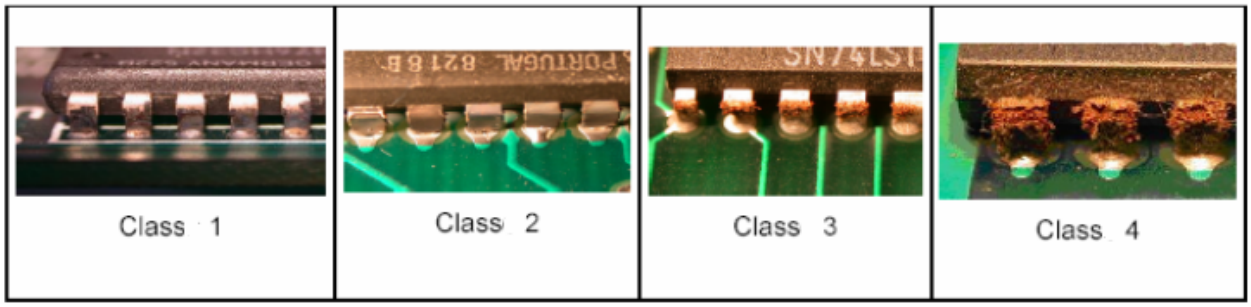

Figure 5-1
Various stages of corrosion.

Logic components in hermetic casings manufactured before 1975 and those manufactured by American manufacturers between 1975 and 1980 may have used Au/Al connections (bondings), the aging of which results in the formation of alloys (the infamous “purple plaque” [14-16]) leading to the separation of the bonding wires. An example is shown in Figure 5-2. All components mentioned here are not necessarily affected by this Au/Al phenomenon but as a precaution, they shall be monitored closely to determine their potential danger, by X-ray examination in particular, which will reveal the nature of the bonding wire (Au or Al) [7].

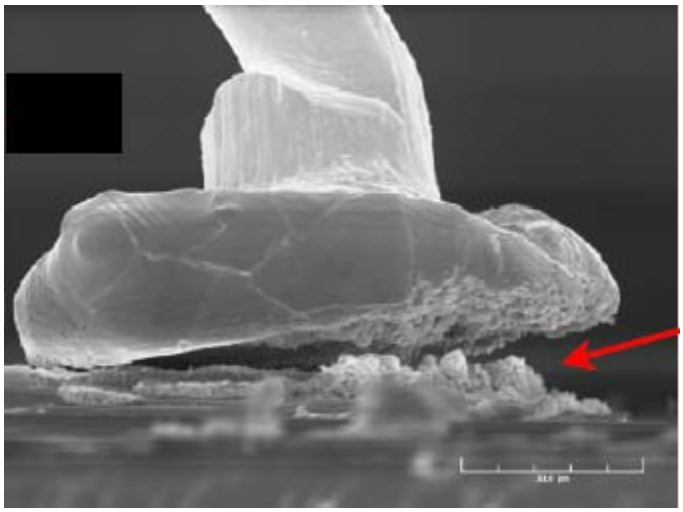

Figure 5-2
Separation of a gold connection wire initially on the aluminum pad of a 2N3019 transistor.

- EPROM memories of the 1980s (types 2516 and 2716 for example). Given the technology used at the time of manufacture, such memories are subject to electromigration. Furthermore, failures may appear if they are reprogrammed too often.
- PROM and SRAM memories in general, which are accessed, show signs of overheating and serious oxide damage during failure analysis.
- Electromechanical or mechanical components (potentiometers, certain relays, etc.), the aging of which depends on the number of times they are handled.

The list above is, of course, not exhaustive. It would be very time-consuming to list components for which a faulty batch has been identified (a specific date-code for a given plant for example), due to a temporary problem in the process. Nevertheless, it includes the main families which are considered to require monitoring.

Sensitive Boards and Systems

On the basis of this list of components sensitive to aging, it is easy to draw up a list of the modules (and by extension systems) sensitive to aging. This involves modules comprised of one or more sensitive components. Therefore, the aim is to determine those systems for which a special effort to monitor aging should be made.

EDF R&D has classified the modules of different systems into three categories:

- A: the module includes at least one type of active component highly sensitive to aging.
- B: the module includes several active components sensitive to aging.
- C: the module contains no active component sensitive to aging.

It is important to note that this classification only takes active components into account. This does not mean that there are no passive components sensitive to aging. The case of electrochemical capacitors has already been discussed at length. However, passive components are considered to pose far fewer problems of replacement than active components since, based on EDF's experience, passive components are easier to get over time and are only in a very few cases obsolete. Due to this, EDF's strategic stock of electronic components is made up almost exclusively of active electronic components.

For information, of systems studied, the percentage of modules in category C varies from 30 to 66%. This rate is not fixed, indeed, it is bound to change as further destructive tests are carried out or more visual inspection campaigns are initiated.

Preventive Replacement and Partial Renovation

Once sensitive components and modules are identified and the causes of failure and rate of operational failures known, it is possible to set up an effective policy of preventive replacement, to limit the number of failures, while doing it at the right time to avoid the preventive replacement of too many components. In addition to the economic aspects of reducing unnecessary preventative maintenance, this is made necessary due to the fact that certain components are obsolete. They cannot be procured and we must; therefore, manage the strategic stock to avoid over-consuming them.

At present, the main preventive replacement operations in progress concern the following families of components:

- Electrochemical capacitors.
- Potentiometers.

- Switches.
- Lithium batteries.
- Relays.

These are mainly passive components and electromechanical components. Thanks to the studies discussed above, active components have already been covered, in most cases.

Preventive replacement is not always possible (clear cases of obsolescence, large number of maintenance operations already carried out, etc.) and the partial renovation of systems considered to be aging is sometimes preferable. All the aging studies described in this report provide input data for making the decision for renovation. Indeed, if the studies show that a system is generally aging quickly, it should be refurbished, putting all other technical (increase in the number of functionalities, etc.) or economic considerations aside.

6
MITIGATION OF EXTERNAL FACTORS

List of the Stressors Concerned

The studies conducted by EDF R&D show that the four main forms of external factors which have a negative effect on the life span and reliability of printed circuit boards are, in decreasing order of importance, handling, ambient conditions, electrical overload and excessive operating temperature. Aging due to radiation is not taken into account. Indeed, it may be said that there are no electronics inside the reactor buildings of French power plants. Accordingly, there is no irradiation of components. The only aging due to radiation to be taken into account is that due to natural atmospheric radiation (due to cosmic particles) and which generates Single Event Effects (SEE). The most common technology in use on French nuclear sites is quite old (20 to 30 years) and is only slightly sensitive to atmospheric neutrons and other associated particles. Nevertheless, it must be pointed out that studies are underway to integrate electronic components in the reactor building in order to take into account that more and more commercial-of-the-shelf (COTS) sensors are fitted with electronics very close to active zone of such sensors.

Handling

Impact of the Human Factor

The human factor is the cause of much of the damage to printed circuit boards, leading to a reduction in life span or the overall reliability of the board. Two findings support this conclusion. First, during a campaign of visual inspections carried out by EDF R&D on 1300 MW units, it was shown that the most severely damaged boards are those which are handled the most (repairs not in accordance with the state of the art, handling with inappropriate tools, etc.). Second, a study carried out in 2002 on electronic components found to be defective in operation revealed that a not inconsiderable part (more than 20%) of failures were due to electrostatic discharges (ESD) (see below). Not all electrostatic discharges are due to a poor handling, but a high rate of ESD suggests that the handling of boards is not necessarily optimal.

General Recommendations

To limit the impact of the human factor on the reliability and residual life span of printed circuit boards, the following recommendations have been made and are reviewed regularly for “automatic control” departments during training courses:

- Limiting the handling of boards: this recommendation is by far the most important, no board should be removed from its rack without a good reason (maintenance or trouble-shooting).

- Systematic use of protection to limit risks due to ESD must be taken (see next section).
- Do not clean boards, except where absolutely necessary: necessary examples are connector clearly fouled, bridge of dust between two component leads, leading to a risk of short-circuiting (see example in Figure 6-1). Aerosols must not be used (composition often unknown and risk of thermal shock for fragile components). The best solution consists in blowing away the dust using a jet of nitrogen under pressure, ensuring that the direction of the flow does not lead to the dust being re-deposited elsewhere. Another solution consists in using a suction device and/or antistatic brushes (thus avoiding any risk of ESD). As a last resort, the operator may use a clean cloth soaked in isopropyl alcohol. The use of any other products, gum, etc. is strictly forbidden.

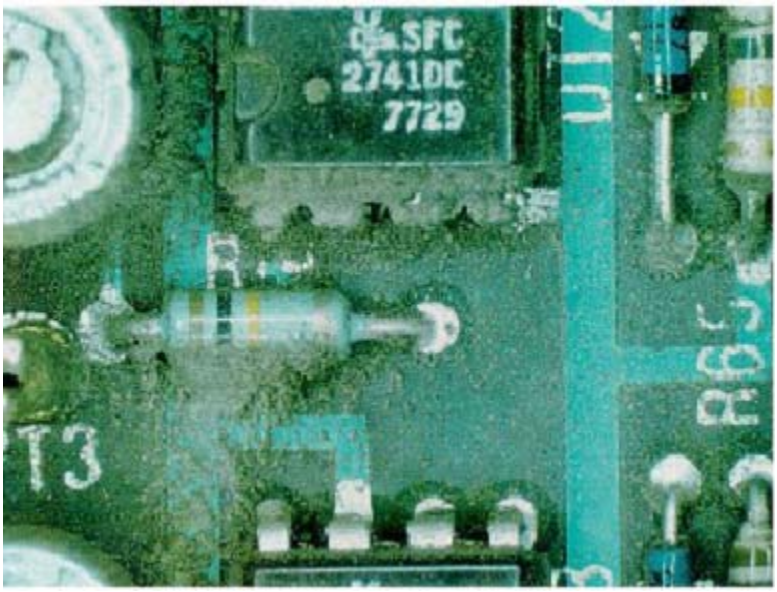

Figure 6-1
Example of a severely fouled board for which cleaning is required.

- Use of appropriate carrying boxes even for just transferring the board on site: all boards must be transported in individual antistatic packaging, as shown in Figure 6-2 (left-hand side), in order to avoid scratches which could cut or lay bare the tracks of the printed circuit (see right-hand side of Figure 6-2) or twist the electronic components.

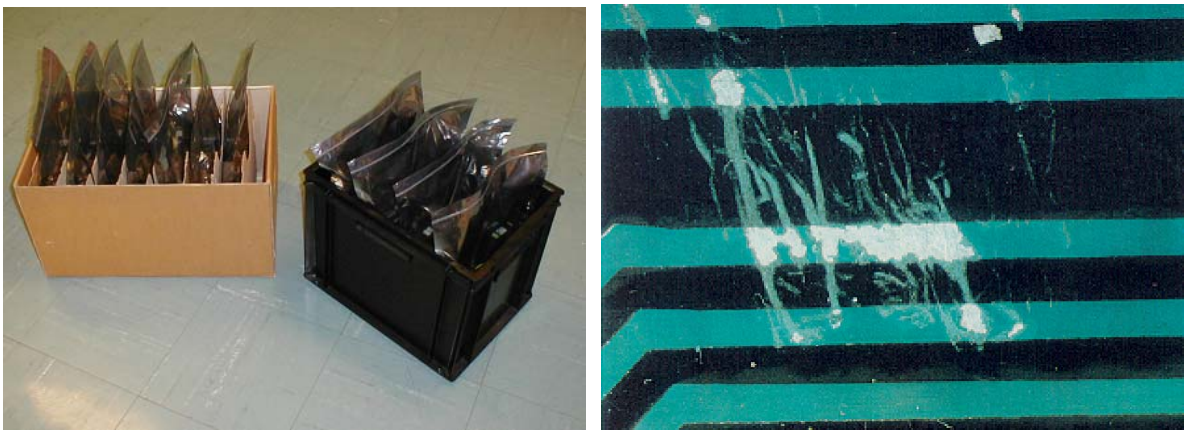

Figure 6-2
(left) Examples of packaging for transporting the boards on site, (right): track of a printed circuit laid bare due to two boards rubbing against each other during transport.

Always unplug boards when de-energized (with the exception of specific recommendations by the manufacturer of the system – example: Alstom Controblock). Unplugging energized leads to the appearance of intense arcs of varying durations and the cooking of contacts or even vaporization of the conducting layers of power contacts. An example is given in Figure 6-3.

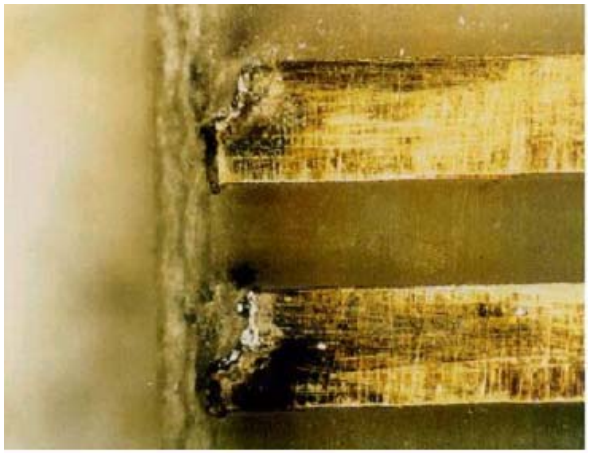

Figure 6-3
Connector unplugged while energized.

- Systematic check of the state of the male connector (on the board) before any connection operation must be done.
- It is forbidden to straighten a board that is out of shape or a twisted connector: in most cases, the connector (or board) is in plastic distortion. Accordingly, straightening will at best result in permanent mechanical stress and, at worst, mechanical failure.
- No direct contact with the edge-board contacts of a connector. As mentioned above, connectors, especially card-edge connectors, are highly sensitive to pollution, in particular organic pollution. A simple contact with a bare edge-board contact brings moisture (from sweat) and fragments of dead skin, etc. or even food residues. The presence of compounds

probably from citrus fruit in the contact area has already been detected during inspections of connections.

- Systematic use of appropriate tools must be taken, particularly during the reprogramming of EPROMs (Erasable Programmable Read Only Memory). Figure 6-4 shows damage to a potential strip due to the use of a non-conventional tool (in this case a screwdriver) to remove an EPROM from its slot. The use of inappropriate tools may also lead to scratching of the printed circuit, resulting in loss of electrical continuity in the tracks of the PCB or in them being laid bare, eventually causing oxidation and/or corrosion of tracks.

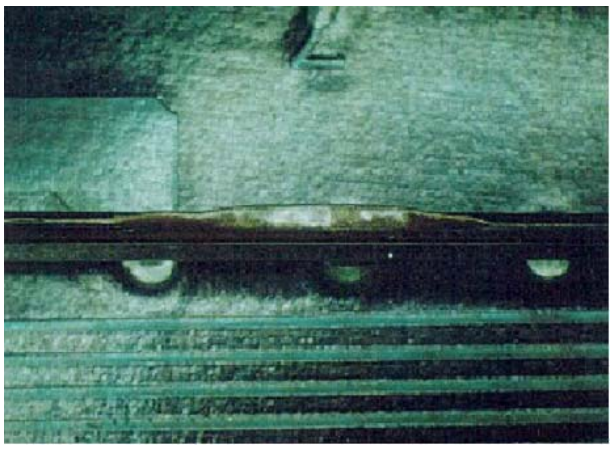

Figure 6-4
Potential strip damaged by the use of inappropriate tools.

General Recommendations

The most important recommendation aimed at limiting the impact of handling undoubtedly concerns the fight against electrostatic discharges (ESD). We must always be aware that the protection against the risk of ESD must be done at all times. The protection should be permanent and the personnel should be trained to use appropriate tools. Indeed, a single electrostatic discharge may be enough to damage a component irretrievably, without the operator necessarily being aware that he has applied an electrostatic discharge to the board he is handling. This state of affairs may be explained by two phenomena. First, ESD may not be violent enough to cause a failure, but it may lead to embrittlement which will drastically reduce the life of the component affected. An example is given in Figure 6-5. Second, the threshold of human perception of an electrostatic discharge is approximately 2 to 4 kV. Below this value ESD is not felt, yet many technologies are badly affected at this voltage level, as shown in Table 6-1 taken from IEC-61340-5-2. This table clearly shows that not all technologies are sensitive to the risk of ESD to the same extent. Nevertheless by default, we should consider that for all boards, the risk of ESD is not negligible and all useful protections should be taken.

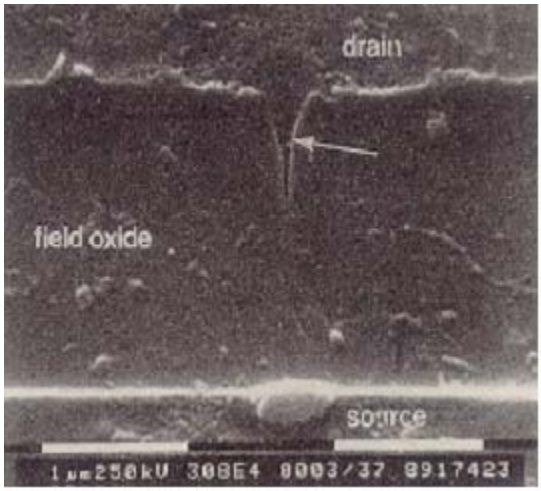

Figure 6-5
Example of partial damage to a transistor following an electrostatic discharge. The component is still functional but the thickness of the oxide is so reduced that failure is close.

Table 6-1
Sensitivity of various component technologies to electrostatic discharges.

Type of Technology	Sensitivity Threshold (V)
MOSFET	100 – 300
MOS VLSI (before 1990)	400 – 1000
VLSI (after 1990)	1000 – 3000
HC	1500 – 3000
CMOS	1000 – 5000
Linear MOS	800 – 4000
Previous generation bipolar	600 – 6000
Modern bipolar	2000 – 8000
Bipolar power components	7000 – 25000
Film resistors	1000 – 5000

Over the last ten years, EDF has extensively developed the fight against ESD within the “automatic control” departments of nuclear power plants. The following measures must be applied continuously, whether the electronic circuit board is a) installed in a rack or frame and b) in operation or not:

- The operator must always be earthed with a resistive bracelet (with a resistance value that is sufficiently high to allow for the slow dissipation of charges and; therefore, a low current passing through the electronic component) according to the applicable standards, typically

1 megohm• (some others have 10 megohms). The total resistance between the ground and the board (including the human body and skin resistance) has to be lower than 35 megohm.

- All system cabinets should be equipped with a central grounding point to which the operator must be connected through the use of a wristband. The value of the resistance to the ground should be checked regularly.
- When a circuit board is being inspected (e.g., inside a cabinet or on a table), it should be laid on an antistatic surface (i.e. for dissipation of charges and connected to the ground by a resistance as above). This does not mean that the operator must not still be earthed as described above and shown in Figure 6-7. Another acceptable approach is for the wristband to have its own path to ground.

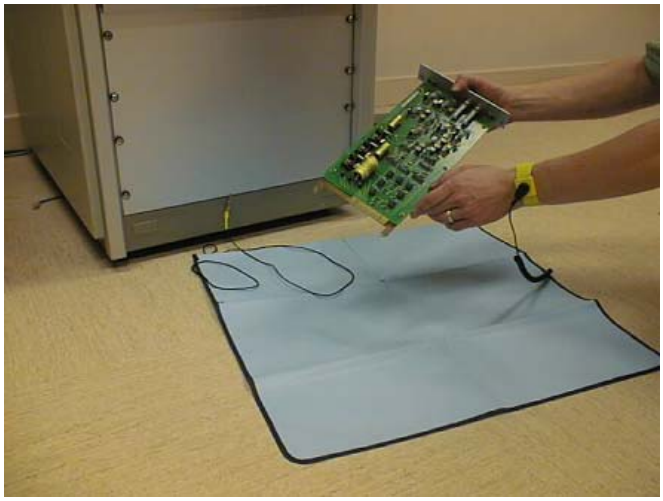

Figure 6-6
Work station for the inspection of printed circuit boards: the operator is connected to the mat which is connected to the grounded frame of the cabinet.

- When transporting boards (from the instrumentation and control cabinet to the testing area for example), packaging that dissipates the charges must be used.

Special care must also be taken with the equipment used to counter ESD. Not all equipment is as efficient as it should be. For transport, in particular, preference should be given to use of protection made of carbon black (bags, strips, etc.). Charges are dissipated inside the protective packaging. Therefore, even in the event of surface wear (due to board rubbing in the antistatic bag for example), the protection remains efficient. Therefore, we must avoid using protection that consists in applying a coating that dissipates the charges to the surface. This is particularly true of pink or brown antistatic bags and translucent strips. Figure 6-8 shows carbon black protection devices.

Figure 6-7
Carbon black anti-ESD protection devices.

Another recommended approach consists in building anti-ESD protection into the design of boards. It should be noted that this recommendation can only apply to newly designed boards since it is not possible to easily apply protection to existing systems. The current approaches for anti-ESD protection are based on thyristors and other components (at the board level) that drive the energy of the ESD to the ground. These protections are not destroyed by an ESD event; even after many ESD events the protection is still active.

Ambient Conditions

Types of Protections

One of the external factors to be taken into account is the ambient conditions. The following are mainly taken into consideration, the rate of humidity and marine atmosphere, especially for the nuclear power plants beside the sea. Depending on the location of the power plant, we must also take the presence of chemical stressors (proximity of large urban areas, polluting factories, etc.) into account. Therefore, we must either control air quality or protect the electronic circuit board from the consequences of atmospheric pollution. If the air quality is good enough, it is not necessary to protect the boards. If not, the protection of the PCB is mandatory (actually it is usually easier to protect the board than it is to control the air quality). Three solutions may be envisaged, depending on the location the protection is to be applied:

- Protection of instrumentation and control rooms: the monitoring of air quality must involve the installation of particle traps and filters for the type of pollutant concerned to control the air circulating in instrumentation and control rooms. A more total solution involves the use of air-conditioning and dust-free environments (clean rooms being particularly unrealistic). However, this solution is not the most effective. Indeed, given the volumes of the rooms and the frequent movement of maintenance personnel, it is unrealistic to try for perfect filtration of the air. Furthermore, we cannot avoid the presence oxygen, moisture and salt in the air, which will make oxidation or even corrosion possible.
- Protection of instrumentation and control cabinets: two measures may be considered in cabinets. First, filtering the air on the air intakes of cabinets to prevent the ingress of dust which could be deposited on the boards and electrical contacts. Second, in order to overcome

aggression due to the presence of oxygen, it may be possible to flush instrumentation and control cabinets with nitrogen, as is the practice for the strategic storage of electronic components. Nevertheless, this solution poses more problems than it solves. First, protection is very complex and costly to set up. Second, the number of interventions on cabinets must be limited to the strict minimum (the more a cabinet is opened, the less effective flushing with nitrogen). Third, unlike boards in storage without power, the boards of instrumentation and control cabinets are under power. This means that the dry atmosphere obtained thanks to nitrogen flushing will increase the risk of electrostatic discharges. Finally, we must provide safety equipment for technicians required to work in the cabinets, where there is a possible risk of anoxia. It must also be pointed out that at present no long term operating experience has yet confirmed the benefits of storing components in nitrogen, as opposed to storage in air.

- Protection of printed circuit boards: a last possibility consists in providing protection on the board itself. The idea is to protect it against external atmospheric attack by the systematic application of varnish once the board has been assembled. The main advantage of the varnish is that it provides a barrier that is potentially airtight to the atmosphere and; therefore, to oxygen, water, salt and the other pollutants and contaminants it contains. Varnish may also provide electrical insulation (although only moderately efficient) between the solders and leads of components. Accordingly, it limits the risk of short-circuiting in the event of deposition of metal or conducting particles on the surface of the board. Another advantage lies in the fact that varnish may provide (depending on the type) good protection against whiskers. While varnish does not prevent the growth of whiskers, it controls the direction of their growth and seals them inside a shell that is difficult to cross. On the other hand, the presence of varnish implies constraints, the main of which concerns repairs. It should be possible to remove the varnish to be able to repair components or the printed circuit, easily (and safely for the electronics). Furthermore, the protection of board is not complete, in particular, connections cannot be protected by varnish since, a semi-permanent contact (card-edge, plug in connectors, etc.) consists in bring together two, bared conducting parts. Aging of connections related to the presence of pollutants has been detected [2]. Finally, varnish will also act as thermal insulation, which will limit the cooling capacity of boards through the exchange of heat with the ambient air. The varnish to be applied must be selected carefully. This aspect will be described in greater detail in the next section.

Types of Varnish

There are four main groups of varnishes conventionally applied to printed circuit boards:

- Acrylic-based varnishes: These varnishes are easily available. Their main properties are that they are relatively flexible and stable (but generally less than polysiloxane-based varnishes). These varnishes are considered to be the best seals. They are used for various applications, not only in electronics (construction, paint, motor industry, etc.) since they have no specificities or specific physical properties in relation to others. In terms of polymerization, these varnishes polymerize at ambient temperature, from several hours to several days and are very easily to apply.
- Polyurethane-based varnishes: polyurethane is a polymer based on urethanes. Urethane has been known since the 1930s (discovered in Germany by Otto Bayer) and was studied in great detail in the 1950s, which explains the large number of applications used at present. In

electronics, polyurethane-based varnishes are particularly recommended to combat tin whiskers. Indeed, polyurethane-based varnishes are very rigid and provide an efficient barrier against the growth of whiskers (whiskers grow inside the film of the polyurethane that is very difficult to pass through). Protection against moisture is also one of the reasons for the use of these varnishes. Nevertheless, their hardness is their main disadvantage. During polymerization or variations in temperature (during their life span, for example), it is not rare to see the appearance of cracking. Therefore, the durability of the barrier provided by these varnishes is not among the best. Furthermore, they do not follow the geometry of the surface on which they are applied, which results in variations of thickness from the very outset.

- Varnishes based on polysiloxane (better known as silicone): these are inorganic compounds (unlike polyurethane), based on the chemistry of silicon and more particularly on chains of Si6O bonds. Organic groups may be used to bond groups of Si6O links, which results in widely differing geometries and physical properties. In general, the properties of silicone based varnishes are very different to those of polyurethane varnish. Chemically, they are very stable (thanks to the strong Si-O bond) and their properties are stable in time. Once polymerized, these varnishes remain flexible; allowing them to match the contour of the parts varnished perfectly and tolerate deformations due to thermal cycling (day/night, summer/winter, etc.). These varnishes are considered to be the most durable. They resist moisture quite well, but in general less than acrylic and polyurethane- based varnishes. It must also be pointed out that like polyurethane-based varnishes; these varnishes polymerize at ambient temperatures around 70 to 90°C.
- Parylene-based varnishes: parylene is the generic name given to a family of polymers, simplest representative of which is poly-p-xylylene – or parylene N – discovered in 1948. Parylene may be applied in very fine coats. It retains its dielectric properties even for coats of less than 1 µm. Furthermore, the film deposited is continuous and damp-proof (moisture absorption is approximately 10 times less than that a silicone based varnish) [17]. Durability in air at 100°C is 100.000 hours, or approximately 10 years. The main disadvantage of parylene is due to its method of application. Using the Gorham's process [18], a precursor (often a derivative of paracyclophane) is placed in a low vacuum (0.1 Pa) and heated to more than 100°C to be sublimated. The vapor recovered is heated to a temperature of between 500 and 700°C to break the aliphatic C-C bonds and obtain monomers of p-xylyylene which are sent to the deposition chamber and which polymerize naturally by deposition on the surface to be varnished. This process is difficult to apply and patents have been filed. Accordingly, parylene coating is only carried out by a few companies in Europe; the largest use appears to be in the United Kingdom. This is due on the one hand, to the need to transport and handle boards (which is not recommended, especially for boards which are already weakened) and on the other, to a risk due to the availability of deposition installations without alternative solutions.

Given the properties of the varnish, it would appear that a parylene-based varnish is by far the most satisfactory. However, the difficulty of application results in it not being used since it is impossible to apply on site, limited number of operators capable of applying it, difficult to remove, etc. Therefore, we recommend the use of polyurethane-based varnishes. They are easy to apply and remove using ad hoc techniques (etching or sand blasting). They are also the most efficient solution against whiskers [19], oxidation and corrosion. This has been shown clearly by studies conducted by EDF R&D. Iron and iron-nickel alloy (easily corrodible) bars were coated with various varnishes (acrylic, polysiloxane and polyurethane) and exposed to a standard saline

mist (5% weight of NaCl in water, at a temperature of 35°C) for 96 hours. It is clear that the resistance of polyurethane-based varnishes is greater than the others, as shown in Figure 6-9.

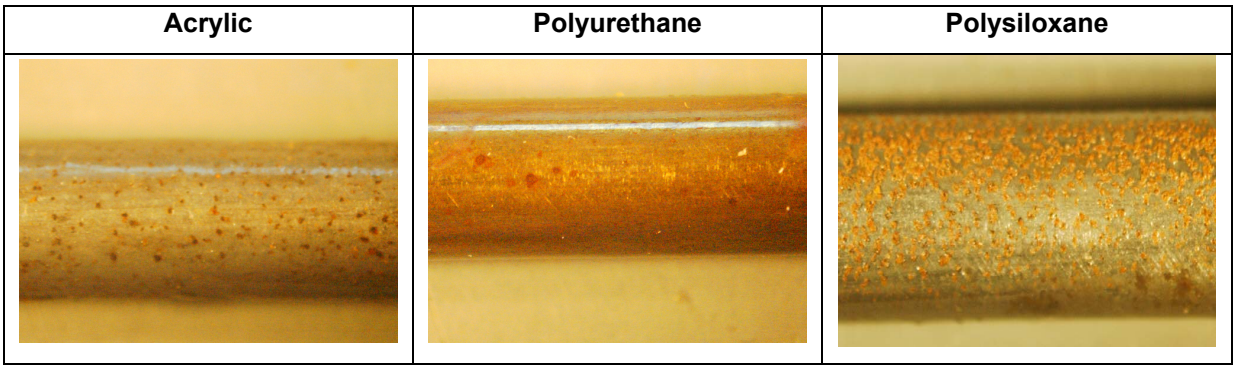

Figure 6-8
Comparison of the permeability to corrosion of three varnishes (acrylic, polyurethane [orange] and polysiloxane): we observe less pitting in polyurethane-based varnishes.

Conclusions

The mitigation of stresses due to ambient conditions must involve the application of varnish, preferably polyurethane-based varnishes, on printed circuit boards after assembly. However, this is not sufficient to protect connections from problems of foreign particles between the two parts of the connectors and from oxidation.

Electrical Overloads

The last type of stress to be taken into consideration is voltage or more exactly over voltage, which will cause an electronic component to operate outside its technical specifications (current and/or voltage too high) for a certain time. The origin of this stress is generally the failure of another component which stores energy (typically a capacitor) or a problem with the power supply of the board. There are virtually no means of protecting against electrical overloads, especially for those where the cause lies on the same board as the component to be protected. The only effective method lies in the use of protection by design and, in particular, the use of shunts, peak detector or protective diodes. Nevertheless, such protection is not the most effective. No other type of protection is currently used on instrumentation and control systems by EDF.

It is recommended, as a preventive measure, to backfit power supply modules on a regular basis and, in particular, to ensure that no component that stores power fails (typically, by regularly replacing electrochemical capacitors, the life span of which is limited). This will limit the risks of overloads but does not eliminate them completely.

Operating Temperature

Operating temperature is an important parameter that must be controlled. It can be seen by applying an Arrhenius type aging model with standard activation energy of 0.7 eV, an increase in temperature of 10°C reduces life span by 50%. Nevertheless, problems of failure due to high temperatures are still quite rare.

EDF has not yet opted for the air-conditioning of premises housing instrumentation and control cabinets. Other measures have been taken to limit the temperature inside cabinets; in particular cabinets are cooled by air flow.

It is not enough to monitor the temperature of cabinets to ensure that the temperature of components is correct. For example, for an active component, the temperature that results in aging is the temperature of the chip and not ambient temperature (although both are linked by various thermal resistances, in this case, the casing, mechanical connections, etc.). Since thermal resistances are generally quite well known, we can determine the operating temperature of the component by measuring the temperature of the casing. For this, heat-sensitive pads are used locally. Once affixed to the casing, these pads are left in place for several weeks and they indicate the maximum temperature to which they have been exposed. This enables us to determine the temperature of a component and whether corrective action should be taken if the temperature measured is too high. It may be that the cause of the component overheating is internal (aging), but it may also be due to an external cause such as from the wrong power component in the vicinity, air flow insufficient for cooling, etc.

At present, this form of monitoring is sufficient.

Special Case of the Storage of Electronic Components

The recommendations above concern printed circuit boards in operation. They should also be applied, without exception, to boards in storage and, in addition, the following instructions shall be followed:

- Regulation of temperature at about 20°C.
- Regulation of humidity at about 35%. This value is, in fact, a compromise between the need for a high rate of humidity to limit the risk of electrostatic discharges and the need for low humidity to limit corrosion and the “pop-corn” effect during the assembly of the components stored alone (i.e., not soldered on to the printed circuit). For information, the pop-corn effect is due to moisture absorption by the packaging of the component. If during assembly the component has not been properly dried, water (initially in liquid form in the packaging) vaporizes and causes cracking.
- Storage of components in hermetic cabinets with a single ground to earth, to limit the risk of ESD still further.
- General use pf the anti-ESD protection devices such as those described in French standard NF EN 61340-5.

- Forbidding the use of single use packaging (see above). If components are delivered in such packaging, they should be repackaged using long term protections, i.e., carbon black packaging.
- Use of packaging that allows air to circulate to limit the consequences of degassing. For the same reason, cardboard boxes shall be prohibited in storage areas.
- Replace packaging of the type “dry-pack” which has a limited life span, on a regular basis.

At present, no recommendations have been made concerning the gas in which components should be stored, either air or nitrogen. For the moment, nothing suggests a preference for one or the other.

Conclusions about the Mitigation of Stressors

According to the discussions above and if only three main good practices were to be retained, EDF R&D recommends strict compliance with the following recommendations:

- Systematic use of anti-ESD protection, even when the board is supposed to be immune to all risks.
- Limiting the number of times printed circuit boards are handled to an absolute minimum, including restrictions as to the types of maintenance operation authorized (particularly for the cleaning of boards).
- Systematic varnishing of boards, preferably with a polyurethane-based varnish following the assembly of boards.

These good practices alone will prevent a large number of failures due to external stress. In particular, according to the statistics gathered by EDF R&D between 2002 and 2005, they prevent approximately 15% of the failures recorded over this period.

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ASPECTS TO BE DEVELOPED

In order to take the analysis and anticipation of aging further to find a better approach for maintaining operational conditions, three additional aspects should be examined. They are the use of built-in sensors for continuous monitoring of a board's environment, on-line analysis techniques and looking for early warning indicators of aging.

Environment Monitoring Micro-Sensor

During failure analyses, the analyst often lacks information as to the real conditions experienced by the board or component in front of him. He relies on an average mission profile in trying to find the causes of damage without knowing the real operating conditions of this particular board (actual operating time, temperature extremes encountered during the life of the board, presence of stresses such as overloads (electrical overstress (EOS)) or electrostatic discharges (ESD), etc.).

The aim of a study now underway with EDF R&D is to successfully develop a micro-sensor capable of measuring as much data as possible concerning the direct environment of boards and with the following information at least, at the same time:

- Service life.
- Temperature.
- Electrical field (in order to detect events such as EOS and ESD).

Other measurement functionalities may of course be added but do not take priority (detection of shocks, etc.). The idea is to succeed in developing a sensor that is sufficiently compact to be able to integrated on any board (current or new) and to achieve the desired information with only one sensor per board. The development of such a micro sensor still requires considerable R&D effort, particularly in terms of questions concerning its electrical power supply and qualification.

In the long term, it is also hoped that such a use of this system will prevent failures such as those due to EOS-ESD. Indeed, if the sensor detects detrimental phenomenon, it could inform the operator who will be able to take appropriate action. As mentioned above, the consequences of ESD are not necessarily visible directly and such a sensor would help to anticipate them.

On-Line Analysis Techniques

Another important thing to have for the maintenance of systems is the possibility of carry outing tests on-line. As discussed above, most of the analyses developed by EDF R&D are destructive

in nature. Certain non-destructive tests are also possible, but only off-line to limit the impact of measurements on the system. Ideally, we should have measurements on-line, in the same way as periodic testing, which would give us continuous monitoring of the aging of printed circuit boards.

This point is important and the effort required should be considered to be a priority. However, it will be difficult to set up detailed on-line analysis capabilities for existing boards. Therefore, it is preferable to concentrate efforts on new or refurbished installations.

Early Warning Indicators of Aging

The last point requiring additional investigations is the search for early warning indicators of aging. The earlier a failure mechanism is detected, the quicker the required action to prevent this failure may be taken. This necessitates in particular detecting, by non-destructive means (typically a low current electrical measurement), the variation of a particular parameter (to be defined according to the type of component and mechanism concerned) that could indicate the start of aging. These studies are time consuming since there are no generic methods applicable to each component, whatever the technology and failure mode of interest. The technique adopted consists in studying aging behavior which is accelerated to determine an aging equation, family by family of components. This is what was done for capacitors for example, and what should be done for other components considered to be sensitive to aging (such as memories).

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CONCLUSIONS

This report has revealed a number of good practices recommended by EDF. The most important ones may be broken down into three groups:

1. Determination of the state of aging of installations:
    - Regular (or even systematic) visual inspections when a board is handled.
    - Regular check of the aging of sensitive components for which we have more elaborate diagnostics tools (capacitors, thyristors, optoelectronic couplers, etc.).
    - Systematic destructive testing of defective active components.
    - Looking for signs of aging on components and solders by non-systematic destructive testing.
    - Monitoring of reports from PCB repairers.
    - Monitoring good practices from other industrial concerns.
2. Developing lists of components sensitive to aging and drafting a maintenance strategy:
    - Definition of levels of sensitivity of components and modules to be reviewed according to any change to the aging status observed previously.
    - Preventive replacement on the completion of these studies.
3. Mitigation of external stresses, including:
    - Developing a guide of good practices for the handling of printed circuit boards to limit stresses caused by humans.
    - Limiting the number of handling operations.
    - Systematic use of anti-ESD protection.
    - Varnishing of electronic circuit boards with polyurethane or silicone varnish.

All these recommendations improve our knowledge of aging, the anticipation of failures and the mitigation of external stresses. Despite this level of control, improvements still need to be made and are being studied by EDF R&D.

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REFERENCES

[1] M. El Hadachy, et. al., Thèse de l'Université de Monpellier II (2008).

[2] L. Crétinon, et al., "Influence of the organic pollution on the reliability of HE9 connectors," Microelectronics Reliability, 48, 8-9, pp. 1129-1132 (2008).

[3] G. Guffroy, et al., "Impedance microscopy on aluminum and tantalum capacitors after more than 10 years in use at EDF," Proceedings of the CARTS-Europe conference (2003).

[4] N. Xiong, et al., "Tantalum capacitors failure diagnosis using computer-aided frequency analysis of the impedance," Proceedings of the CARTS-Europe conference (1990).

[5] Y. Ousten, et al., "Frequency analysis applied to passive component as tantalum, aluminum or ceramic capacitors," Proceedings of the CARTS-Europe conference (1999).

[6] G. Simon, et al., "A pragmatic methodology for the monitoring of the component aging: the case of power thyristors at EDF," Microelectronics Reliability, 38, 6-8, pp 1361-1366 (2001).

[7] L. Crétinon, et al., "Benefits of failure analysis and destructive physical analysis," Proceedings of the HMIT-NPIC conference (2010) – To be published.

[8] K. Nikawa, S. Tozaki, "Principles novel OBIC observation method for detecting defects in Al stripes under current stressing," Proceedings of the 19th International Symposium for Testing and Failure Analysis (ISTFA), 303 (1993).

[9] J. S. Hwang, "Environmental friendly electronics: lead-free technology," Electrochemical publications, Isle of Man, p. 464.

[10] W. Engelmaier, "The changeable structure of solder joints," Global SMT & Packaging, 4, 1, 31-32 (2003).

[11] L. Crétinon, "Maîtrise des réparations mixtes SnPb-RoHS," Proceedings of the 9ème Congrès International Brasage – Brest (2010).

[12] A. Crosson, et al., "Long term reliability of silicon bipolar transistors subjected to low constraints," Microelectronics Reliability, 47, 9-11, 1590-1594 (2007).

[13] A. Crosson, thèse de l'Université Paul Sabatier – Toulouse I (2009).

[14] E. Philovsky, "Intermetallic formation in gold-aluminum systems," Solid State Electronics, 13, 1391-1399 (1970).

[15] P. V. Plunkett, et al., "Low-temperature void formation in gold-aluminum contacts," 32nd Proc. IEEE Electronic Components Conf., pp. 421-427 (1982).

[16] M. K. Md Arshad, et al., "Characterization of intermetallic growth of gold ball bonds on aluminum bond pads," Intern. Journal of Mechanical and Materials Engineering, 3, pp. 187-197 (2008).

[17] Y. S. Yeh, et al., “Polymerization of para-xylylene derivatives, morphology of parylene N and parylene C films investigated by gas transport characteristics,” Journal of Polymer Science Part B: Polymer Physics, 28, 4, 545-568 (1989).

[18] W. F. Gorham, “A new general synthetic method for the preparation of linear poly-p-xylylene,” Journal of Polymer Science Part A: Polymer Chemistry, 1, 4, 3027-3039 (1969).

[19] M. Kaing, “Evaluation of the ability of conformal coating to inhibit tin whiskering,” Proceedings of the 9ème Congrès International Brasage – Brest (2010).

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