

Program on Technology Innovation: SiC-GaN Optically Triggered Power Device

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EPRI Project Manager R. Adapa

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National Center for Reliable Electric Power Transmission (NCREPT) Department of Electrical Engineering University of Arkansas 2055 S. Innovation Way Fayetteville, AR 72701

Principal Investigators A. Mantooth M. Ware G. Salamo

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ABSTRACT

This project investigated the feasibility of an integrated GaN-SiC optically controlled thyristor. The goals of this project focused primarily on producing a working GaN-SiC device. There were several benchmarks along the way. First, in terms of crystal growth: 1) achieve high p-type doping in GaN for the gate layer of the structure, 2) demonstrate a stand-alone, working p-GaN/n-GaN diode structure, 3) achieve high-quality growth of GaN on SiC, 4) demonstrate a stand-alone, working p-GaN/n-SiC diode structure, and 5) grow n-GaN/p-GaN on n-SiC/p-SiC that was provided by CREE Inc. Further work would include characterization of the photocurrent of the junctions of each of the stand-alone diode structures, including the factory-supplied n-SiC/p-SiC, and ultimately of the final device, demonstrating a photo-induced turn-on of the current. Unfortunately, this study did not yield positive results, and the report indicates that the starting SiC material was too poor to overcome. Recommendations for obtaining better quality material are provided, as well as suggestions for the research that can be conducted for this promising device technology going forward.

Keywords

Diode structure GaN-SiC Optical controls Photocurrent Thyristor

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1 SIC-GAN OPTICALLY-TRIGGERED POWER DEVICE

Project Overview

SiC based high power devices have the potential to demonstrate a much higher level of efficiency than Si devices due to their much higher breakdown fields (more than 10 times) and thermal conductivity (more than double). However, SiC is still limited somewhat by the associated control electronics. It can operate up to and above 400°C, but the associated gate dielectrics still decompose at ~200°C, and packaging has also yet to match the high operating temperatures of SiC. At the same time, the integrated gate in common thyristor designs creates a channel for power loss directly into the control electronics. An all optically-controlled gate would add a tremendous amount of flexibility to these devices allowing them to be used to their full potential. However, SiC is limited in its optical efficiency due to its indirect bandgap.

GaN and its associated III-nitride semiconductor alloys, have been used in a wide range of production LEDs and semiconductor lasers in part due to their direct bandgap. GaN also has electrical and thermal properties which match closely those of SiC. However, bulk GaN substrates have not been successfully developed at a production scale like SiC. A key component of modern high efficiency, high power devices could be realized by the marriage of SiC base structures, with epitaxially grown GaN gates for high power optically controlled devices.

In this project, we have attempted to utilize the strengths of both SiC and GaN together to make an optically-controlled thyristor, shown schematically in Figure 1-1. Specifically, the n-type SiC substrate was obtained from Cree with a p-type SiC film grown epitaxially. The p-SiC serves as the anode, A, then the thick n-SiC substrate is the base. Then, on what was the reverse side of the substrate we deposited p-GaN for the optical gate, and then n-GaN for the cathode, K.

Pending a successful electrical measurement of the device, pulsed laser excitation with energy near the bandgap of GaN would be used in attempt to create an electron-hole plasma sufficient to turn the device on. Further tests to investigate the possibility of turning the device off using subbandgap pulsed laser excitation would be performed subsequently.

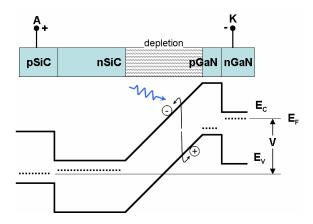


Figure 1-1 SiC/GaN thyristor shown in the forward OFF state with an optically-triggered gate.

Project Goals

The goals of this project focus mainly on getting a working device grown and fabricated. There are several benchmarks along the way. First in terms of crystal growth: 1) Achieve high p-type doping in GaN for the gate layer of the structure. 2) Demonstrate a standalone, working p-GaN/n-GaN diode structure. 3) Achieve high quality growth of GaN on SiC. 4) Demonstrate a standalone, working p-GaN/n-SiC diode structure. 5) Grow n-GaN/p-GaN on CREE provided n-SiC/p-SiC. In terms of characterization, we must characterize the electrical properties (current-voltage curves) of each of the standalone diode structures, including the factory supplied n-SiC/p-SiC. Further work would include characterization of the photocurrent of these junctions and ultimately of the final device demonstrating a photo-induced turn on of the current.

Research Highlights

CREE wafer evaluation

A test wafer was obtained from CREE with the following characteristics: 3-inch n-SiC wafer with a 500 nm thick layer of p-SiC grown epitaxially on the Si face. This surface, shown in topography in Figure 1-2(a), has a well-reconstructed pattern of \sim 20 nm high by \sim 250 nm wide steps which demonstrates the \sim 3.5° miscut of the substrate. However, the C face, shown in Figure 1-2(b), has no regular surface reconstruction and is covered with deep scratch marks. This surface has been optically polished, but scratch removal was not performed. GaN growth was achieved on this surface with only a slight degradation.

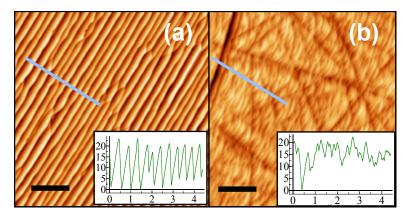


Figure 1-2 AFM of SiC wafer from CREE. (a) Si face with 500nm pSiC grown by CREE. (b) C face, showing polishing scratches. Scale bars are 2 μ m, and each inset shows the grey cross-section. Height axes units are nm and length axes units are μ m.

P-type GaN growth tests

Initial growth tests using a high capacity valved Mg doping cell have produced samples which demonstrate a level of Mg incorporation which is at a nominal level to achieve the desired device structure. The p-type attribute of Mg doping in GaN, however, is nonlinear and converts to n-type for very high atomic concentrations of Mg, which was demonstrated in our initial growths. We are now able to reproducibly grow p-type GaN at a density of $\sim 5 \times 10^{17}$ cm⁻³. However, further optimization of the growth conditions should allow for doping in the range of 10^{19} cm⁻³.

For these test growths and all the GaN growth that follows the following growth conditions were established. The growths were performed in a Veeco Gen II molecular beam epitaxy (MBE) system equipped with a Uni-Bulb RF Nitrogen Plasma source. Before substrates are loaded into the ultra high vacuum (UHV) environment, they undergo standard degreasing by acetone and methanol. Additionally, all SiC substrates were etched in a buffered oxide etch solution of 7:1::H₂0:HF for 30 seconds. The substrates were then loaded into the UHV system and subsequently outgassed at 300°C before being transferred into the growth chamber and heat cleaned at 800°C for GaN substrates and 1000°C for SiC substrates. For growth, the substrate temperature is held at 750°C. For growth on GaN substrates, the Ga and N sources are opened simultaneously and growth proceeds under slightly Ga rich conditions. For growth on the SiC substrates, the Ga source is opened 20 seconds before the N source to wet the surface with Ga. This prevents nitridation of the SiC surface which would create an insulating barrier several atomic layers thick. Nominally, under these conditions, with a N gas flow rate of 0.5 sccm and a RF power of 350W, we achieve a GaN growth rate of 5 nm/min.

Growth and evaluation of vertical GaN pn junction

In order to fully understand the growth of GaN/SiC p-n heterojunctions, we first characterized a traditional GaN p-n junction. Here, a very simple structure was grown with 100 nm of Si doped GaN and 100nm of Mg doped GaN. The substrate for this growth was a GaN template wafer of \sim 5 µm of metal organic chemical vapor deposition (MOCVD) grown GaN on a c-face sapphire wafer. Carrier concentrations were calibrated with Hall measurements achieving electron concentrations of \sim 5×10¹⁸ cm⁻³ and hole concentrations of \sim 8×10¹⁷ cm⁻³. Typical I-V

measurements from this device are shown in Figure 1-3. Here, a reverse bias blocking voltage of ~30-35V is achieved with these very thin layers. This should establish a minimum performance baseline for this particular project, with higher expectations pending optimization.

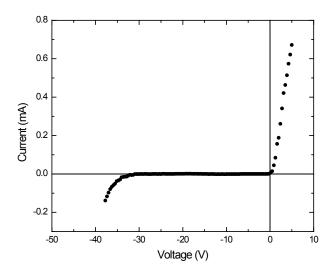


Figure 1-3 I-V for GaN pn junction showing ~35V reverse bias breakdown.

GaN growth on SiC

There is very little published literature on devices which incorporate a GaN-SiC interface into the device structure. SiC has been used very productively for years as a passive substrate in the growth of III-N based structures, however in our work we are attempting to give that substrate an *active* role in the device operation as shown in Figure 1-1. Therefore, the first step in the construction of the GaN/SiC thyristor is to study the electrical characteristics of a single GaN/SiC heterojunction. Figure 1-4 shows an x-ray diffraction (XRD) spectrum of a 300 nm film of undoped GaN on the Si face of an n-type, 4H-SiC wafer. The narrow linewidth of the GaN (0002) peak, FWHM = 133 arcsec, demonstrates the high crystal quality of the growth. This is nearly state-of-the-art for these conditions.

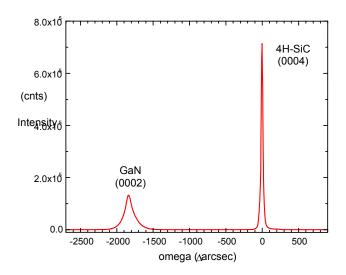


Figure 1-4 XRD showing high quality, FWHM=133", undoped GaN grown on the Si face of 4H SiC.

Growth and evaluation of vertical GaN/SiC pn heterojunction

P-type doping has traditionally been difficult for III-N materials. The most common dopant, Mg, has a very low doping efficiency. Therefore, high levels of Mg are required to achieve, even moderate carrier concentrations. During the course of this project we adapted a high capacity, valved source for the growth of Mg doped GaN material and are now able to achieve carrier concentrations up to ~8×10¹⁷ cm⁻³ reproducibly. This however, comes at a cost to crystal quality as can be seen in Figure 1-5. Here, we grow a 300 nm film of Mg:GaN with a resulting acceptor concentration of ~8×10¹⁷ cm⁻³ on the Si face of an n-type, 4H-SiC wafer. The XRD from the (0002) GaN reflection of this sample has a linewidth of 288 arcsec, more than twice that of the undoped material. This is an indication that the high doping concentration has introduced a significant density of defects into the growth.

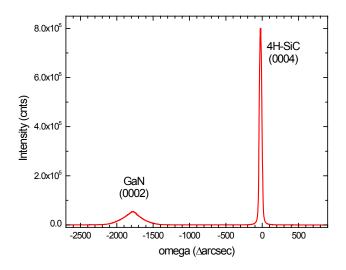
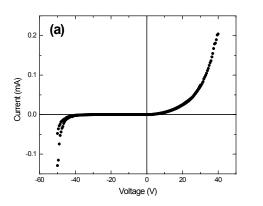


Figure 1-5 XRD showing degradation of GaN quality, FWHM=288", under heavy Mg doping, also grown on the Si face of 4H SiC.

Even though the Mg incorporation has lessened the structural quality of the GaN growth, I-V measurements demonstrate that this device retains significant characteristics of a diode. We find a reverse bias blocking voltage of \sim 45 V, Figure 1-6(a), and a forward turn on in the range of \sim 1 V, Figure 1-6(b), however the device seems to be highly resistive in the on state.



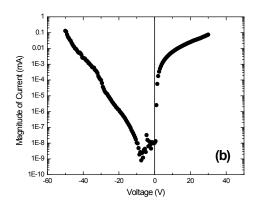


Figure 1-6 I-V for pGaN/nSiC heterojunction. (a) shows the reverse bias breakdown voltage to be \sim 40+ V. (b) is a semi-log plot of the magnitude of the current, which highlights an offset from 0 V in reverse bias which is believed to be due to the band offset of SiC and GaN. Here, it is also evident that the forward bias turn-on is only a few volts, followed by a highly resistive on state.

Thyristor growth and evaluation

Now, with the background of a standalone GaN pn junction and a GaN/SiC pn heterojunction, we can proceed to grow the full thyristor structure consisting of nGaN/pGaN/nSiC/pSiC, where the nSiC is the $\sim 350~\mu m$ thick substrate from Cree with a 500 nm pSiC film grown epitaxially on the Si face. The 500 nm pGaN followed by the 500 nm nGaN growth was performed on the *less desirable* C face of the SiC wafer. In addition to the C face being less well prepared as seen in Figure 1-2(b), GaN growth on the C face of SiC leads to N polar growth, which is also less desirable (than Ga polar growth which results from growing on the Si face) due to the reduced quality of growth which has been found in the literature. Figure 1-7 demonstrates the significantly reduced quality of the GaN grown under these conditions with the large linewidth of the (0002) reflection of 369 arcsec.

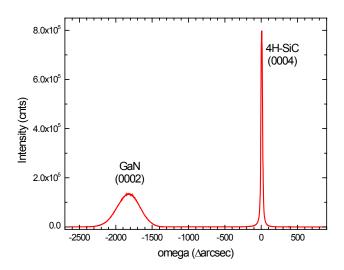


Figure 1-7
XRD showing a significantly reduced quality of GaN growth, FWHM=369", in the full thyristor structure as compared to the single layer of pGaN on SiC. Here the increased intensity is accounted for by the increase in material volume, and the decrease in quality is expected due to the growth being performed on the C face of the SiC substrate.

The electrical characteristics of this device are found to have degraded beyond any useful level with forward and reverse turn on biases of only a few volts, Figure 1-8. We do, however find a small hysteresis in the I-V curve, which may be indicative of the latching action of a thyristor. There are several characteristics of this which make the assignment ambiguous though. First, this hysteresis appears in the reverse bias direction. A hysteresis is expected due to the latching action of the thyristor device in the forward biased, on state. Second, the direction of the hysteresis is opposite that which we would expect from a thyristor. If we consider the hysteresis from Figure 1-8 to be in the forward bias direction, we would expect the trace from an increasing magnitude voltage to have a much lower current than the trace from a decreasing magnitude voltage, due to the latching action allowing a much higher current to pass under a minimal voltage. Here, this is reversed.

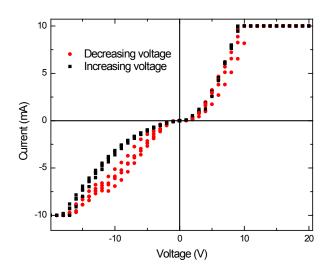


Figure 1-8 I-V for the thyristor structure showing several repeated cycles of the device. This demonstrates a leakage current which is too high to observe the desired thyristor characteristics.

As was stated above in the discussion of the stand-alone GaN pn junction, we expect the characteristics found there to be a minimum performance of the thyristor device, i.e., a ~35 V blocking barrier in the reverse bias, off state of the thyristor. In addition, we have observed the pGaN/nSiC interface alone to achieve a blocking of ~45 V which should appear in the forward bias direction of the thyristor. Therefore, we expect from the characterization of the preliminary devices to have significant blocking on the order of 10s of volts in both forward and reverse bias. As a result, we suspect the starting Cree wafer to be shorting due to existing defects within its bulk. In order to not observe the minimum performance of the GaN pn junction, these defects must have propagated through the growth of the GaN on this wafer.

To test the idea that the substrate was contributing to the bad performance of the device, we performed I-V measurements at different positions on the wafer material which had no GaN growth on it. The results of this testing are shown in Figure 1-9. It is clear that there is a significant inhomogeneity. The material which was used in the study above came from the vicinity of position 2, which we believe explains the poor performance of the thyristor device. Further work could involve growth on material from better regions of this wafer, however even the best response of this wafer is already showing breakdown at ~20 V in the reverse bias direction. So, this is a poor starting point. Better material for the starting substrate must be obtained for this device to reach its full potential.

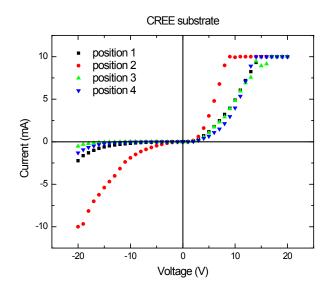


Figure 1-9
IV for SiC pn junction substrate at various positions demonstrating the non-uniformity of the material. Structures grown on other areas of the substrate may achieve the desired characteristics.

Conclusion and Further Study

Throughout the course or this study, several milestones were achieved, which were greatly significant in terms of ramping up a new growth effort to study high power devices based on the marriage of SiC and GaN. Of central significance is the observation of diode characteristics for the growth of pGaN on nSiC. Very little prior work has appeared in the literature on GaN/SiC heterojunctions, and even less for the use of p-type GaN which we believe enhances the performance of these types of devices due to the band alignment between GaN and SiC and the resulting intrinsic field produced at the interface. This successful result opens up a larger field for the use of this material system in that it is not as limited as in the past to only using SiC for the p-type material for these heterojunctions.

The disappointing performance of the full thyristor structure is most obviously the result of a poor quality substrate. While it is generally understood that CREE can produce much higher quality material, it does not seem that it is currently economically feasible for this company to grow the required material needed for this work. Other vendors were pursued in this project but were not responsive to inquiries. For this reason further development on this project might necessitate a university partner who can grow this material on stock substrates. We propose a continuing partnership with funding for another year's work. Approximately \$25k should cover supplies and effort for a partner institution to grow the necessary SiC material, and on the order of \$125k would cover a full time student along with faculty effort and materials at the University of Arkansas to grow and characterize the GaN material and thyristor device.

Assuming an optimized beginning substrate, future work could be more dedicated to studying the SiC/GaN interface, and GaN doping levels. P-type GaN doping has only recently become plausible at higher concentrations. Future work would explore novel techniques of increasing the doping concentration. Currently, there are "tricks" such as Metal Modulated Epitaxy and

polarization doping that have been demonstrated to enhance the doping efficiency. However, current, established growth techniques could be immediately applied to devices grown on high quality substrates to allow for optical testing of the device.

At the same time that the doping levels are being optimized, some attention should be paid to the interface. By the nature of GaN epitaxy on SiC, there will be intrinsic strain in the GaN films. This strain will, unfortunately result in dislocations in thicker films and degradation of the device. Therefore, some research into modified nucleation layers may prove useful in optimizing the device structure, improving its properties and increasing its useful lifetime. Options, such as a thin AlN film may mediate this strain and prevent the formation of dislocations while remaining thin enough to not affect the electrical transport.

Future work would also begin to explore other possible novel power devices based on the SiC/nitride system. The powerful and tunable optical qualities of the AlN, GaN, InN system can allow for the design of intricate optically-triggered power control devices. One can imagine a throttling system controlled by the color of light. Such unique devices can be explored at the same time as optimization to the optically active layer in the thyristor structure is achieved. This final step may include simple approaches such as including a high quality undoped layer in the device to efficiently absorb light or more novel approaches like forming wavelength matched quantum wells to absorb very specific colors of light. This might be matched to current high efficiency LEDs to fabricate integrated optically triggered devices. These are all viable research avenues to pursue.

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