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Technical Update on High-Voltage Direct-Current System Model Development

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Technical Update, November 2017

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ABSTRACT

With increasing integration of renewable energy systems worldwide, there continues to be an increasing consideration given to deploying flexible ac transmission systems (FACTS) such as static var compensation devices, and high-voltage direct-current (HVDC) transmission systems. Because these devices are becoming more prevalent, there is a present need for updated models for system planning studies for FACTS devices and HVDC systems.

EPRI has been a key participant and major contributor in various industry groups such as the Western Electricity Coordinating Council (WECC) Static Var Compensator (SVC) Task Force and the WECC High-Voltage Direct-Current (HVDC) Task Force. In collaboration with these WECC groups a set of three generic Static Var System (SVS) models were developed back in 2011, and have subsequently been adopted and released in the major commercially available power system simulation software tools. Since 2015, EPRI has been working similarly to develop basic planning level models for HVDC technologies. This report provides an update on the finalizing of the line-commutate converter (LCC) based HVDC models developed, which have now been fully adopted, tested and industry approved, and the continued progress of the work on the voltage-source converter (VSC) based HVDC models.

EPRI's participation and active engagement in these broader industry efforts helps to ensure acceptance of the models by all the major stakeholders and that the models are adopted by the commercial tool sets that are used by the utility industry.

Keywords
HVDC modeling
Line-Commutate Converter (LCC)

CONTENTS

LIST OF FIGURES

LIST OF TABLES

1
INTRODUCTION

This report documents the continuation of the work under the P40.016 project from 2016, related to the modeling of High-Voltage Direct-Current (HVDC) transmission systems. The P40.016 project is a broad project covering all aspects of transmission system modeling and model validation. This is one of multiple technical updates associated with the P40.016 project for 2017, and is the report that deals with HVDC model development work.

The main accomplishment for 2017 were the following:

1. Collaborating with the Western Electricity Coordinating Council (WECC) HVDC Task Force and four of the commercial software vendors in North America to bring the work on the line-commutated converter (LCC) HVDC model development work to fruition. The model was finally implemented by four commercial software vendors[1] and thus created the possibility of developing a benchmark test case to be used for testing across the platforms to demonstrate that the model performs as expected and gives similar response across all the software platforms. Subsequently, the model was approved by the WECC modeling and validation working group (MVWG) during its October 2017 meeting.

2. Continued work on the voltage-source converter (VSC) based HVDC dynamic model.

The remainder of this report is organized as follows:

Section 2 summarizes the work done on developing and helping to facilitate testing of the LCC-HVDC simple and standard planning level model, and thus getting the model industry approved.

Section 3 summarizes the continued work relative to the VSC HVDC dynamic model.

Section 4 provides an overall summary, together with a brief outline of the continued efforts in 2018.

[1] EPRI did not fund these commercial software vendors to adopt the model. These entities adopted the model of their own volition and internal funding and thus graciously agreed to test the model in collaboration with EPRI.

2
BENCHMARK TESTING AND FINAL APPROVAL OF THE LCC-HVDC DYNAMIC MODEL

EPRI has been leading the effort for the development of the simple planning level HVDC models under the Western Electricity Coordinating Council (WECC) HVDC Task Force (TF) for the past few years. The WECC HVDC TF is working on developing simple planning models for both power flow and dynamic time-domain simulations in positive sequence software tools for HVDC point-to-point transmission. Models are being developed for both conventional line commutated converter (LCC) HVDC and voltage source converter (VSC) HVDC technology.

The power flow models for LCC HVDC have existed in major commercial software platforms for decades. The VSC power flow model was completed in 2014 [1], and is now available in the main commercial software tools in North America.

In terms of standard and simple planning level models for time-domain dynamic simulation of HVDC, two sets of models are being developed (i) one for LCC HVDC and (ii) another for VSC HVDC. The development, and documentation, of the LCC HVDC dynamic models was completed in 2015, and the detailed specification of this model is covered both in the EPRI 2015 report [2] and publicly on the WECC modeling and validation working group (MVWG) website [3].

At the March, 2015 meeting of the WECC MVWG, it was decided by consensus that the second (*chvdc2*) of the two proposed dynamic model structures for LCC HVDC would be implemented by the commercial software vendors. The commercial software vendors adopt these, and other models, as they are developed at their own volition and cost, and based on user priorities. As such, it took until late summer of this year (2017) for three of the four major commercial software vendors in North America to adopt and implement this model (*chvdc2*) in their tools, ready for testing. In summary,

1. PowerTech Labs has indicated that they have implemented a beta version of both *chvdc1* and *chvdc2* (i.e. both simple LCC HVDC models) in their tool TSAT,
2. PowerWorld has implemented the *chvdc2* model in their tool Simulator,
3. GE has implemented the *chvdc2* model in their tool PSLF, and
4. Siemens PIT, as of November 2017, had almost completed implementation of the *chvdc2* model, with a plan to finalize and release the model by year end.

As such, in late summer we developed a test system and proposed test cases to test the *chvdc2* model in all the various software platforms. The details are presented here, and for the benefit of the public and future software vendors who may decide to also adopt the model, the description of the test case and results were also disseminated publicly through the WECC HVDC TF [4]. The results of this testing work, presented below for completeness, illustrate that the model functions well and as expected and gives very similar, if not exactly the same, results across three of the four commercial software platforms. As mentioned above, the fourth software vendor is presently

working to complete the model in their tool and to run these same tests to ensure they can achieve the same results also. This was all presented at the October 2017 meeting of the WECC MVWG, and subsequently the model was approved by the WECC MVWG and is now available in GE PSLF, PowerWorld Simulator and PowerTech Labs TSAT, and soon to be released in Siemens PTI PSS®E. It is also now on the WECC approved modeling list[2].

2.1 Test Procedure for the CHVDC2 Model

A simple benchmark test case system, based on the CIGRE benchmark case [5], was developed for testing the model. The data for this test case is provided below.

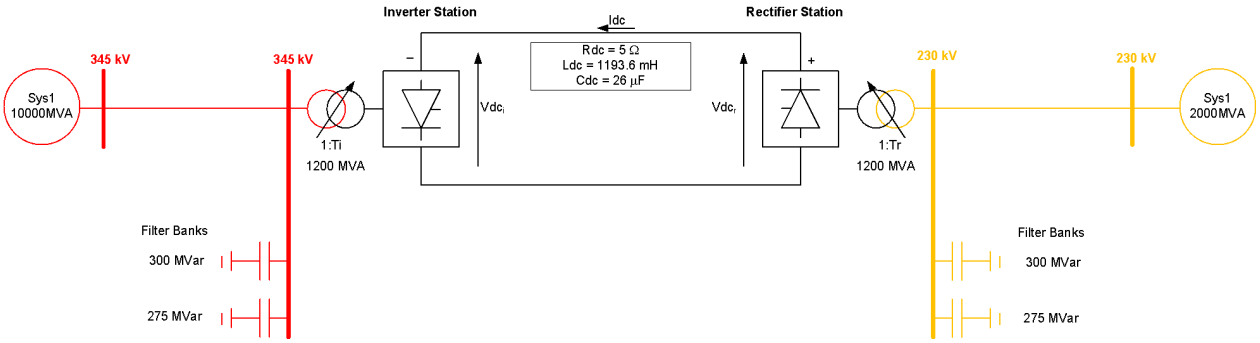

Figure 1: Simple CIGRE benchmark case.

Main Circuit Data

R = 5 Ω, L = 1193 mH, C = 26 µF

V = 500 Vdc, I = 2000 A

Each converter has 2 bridges

Power Flow and Dynamics Data:

The power flow data and solution are shown in Table 1, and Figure 2 and Table 2, respectively. The dynamic model parameters are given in Appendix A. The two classical generators at Bus 1 and 4 are identical and modeled using *gencls*, with the following parameters: MVA = 10000, H = 999999, D= 0, Ra = 0 and X''d = 0.18

[2] https://www.wecc.biz/Reliability/Approved%20Dynamic%20Models%20October%202017.pdf

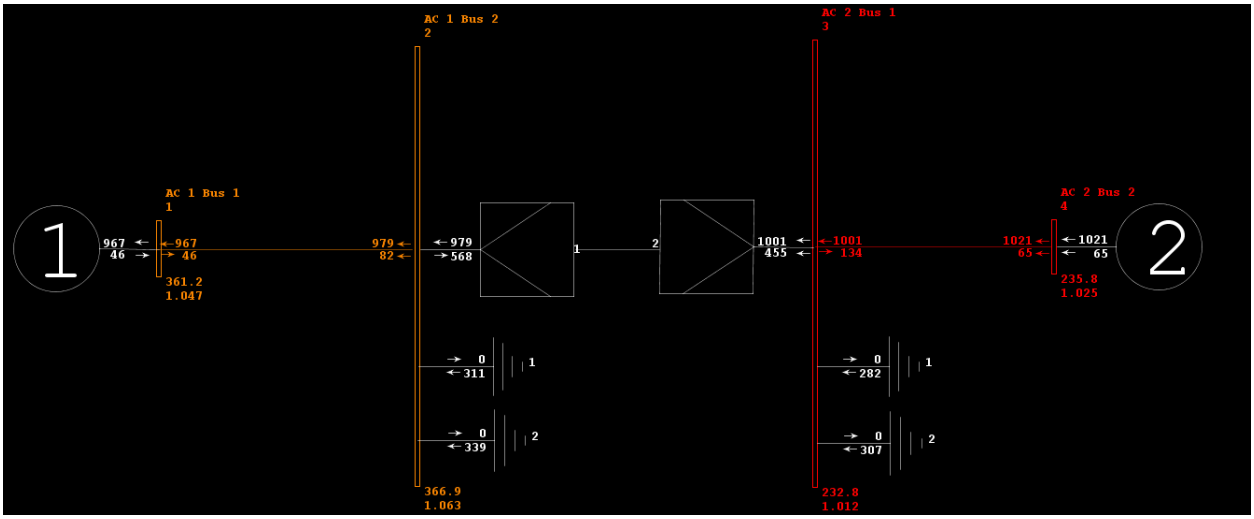

Figure 2: Test case power flow solution.

Table 1: Power Flow Data for the Converters

Parameter	Rec	Inv
Vdiode (per bridge) kV	0.01	0.01
Xcomm (per bridge) Ohms	6.7	6.7
Rtran (per bridge)	0.0036	0.0036
Xtran (per bridge)	0.18	0.18
Vbase AC kV	230	345
Vbase DC kV	211	211
Xfmr MVA	1200	1200
Fxd AC Tap	1	1
Fxd DC Tap	1	1
Adj AC Tap	1.05	1.07
Adj DC Tap	1	1
tap min	0.95	0.93
tap max	1.05	1.07
tap step	0.01	0.01
Max V	0.9	0.9
Min V	1.1	1.1
Xsmooth (mH)	100	100

Table 2: Power Flow solution

BUS-NO	NAME	KV	TP	VSCHED	V-PU	DEG
1	AC 1 Bus 1	345	0	1.047	1.047	-3.98
2	AC 1 Bus 2	345	1	1.048	1.0634	3.54
3	AC 2 Bus 1	230	1	1	1.012	-11.28
4	AC 2 Bus 2	230	0	1.025	1.025	0

BUS-NO	NAME	KV	ID	ST	P	Q
1	AC 1 Bus 1	345	1	1	-966.5	46.1
4	AC 2 Bus 2	230	2	1	1020.6	64.8

BUS-NO	NAME	KV	CNV BUS	NAME	KV	ID	ST	TYPE	PSCHED	IDC SCHD	VDC SCHED	PAC	QAC	IDC	VDC	ALPHA	GAMMA	ALPH MIN	GAMMA MIN
3	AC 2 Bus 1	230	17	DC Rec	422	2	1	REC	1000	2000	500	1000.7	454.6	2000	500	16.87	15	5	15
2	AC 1 Bus 2	345	18	DC Inv	422	1	1	INV	0	2000	500	-979.3	568.2	2000	490	15	24.45	110	18

The *chvdc2* dynamic model data is presented below in Table 3.

Table 3: CHVDC2 Dynamic Model Parameters

Parameter	Value	
dcbusr	17.000	
dcbusi	18.000	
MW_base	1000.000	
Talpr	0.020	
Kir	20.000	
Kpr	10.000	
alpha_max_ram	30.000	
Tram	0.100	
Vram	0.850	
Ttram	1.000	
maxc	0.015	
minc	-0.050	
rmax	10.000	
rmin	-10.000	
Tr	0.010	
Talpi	0.020	
Kii	20.000	
Kpi	10.000	
Kcos	0.070	
Kref	3.000	
Tref	0.010	
Kmax	0.150	
Tmax	0.010	
cosmin_i	0.956	
Imax1	0.100	
Imax2	1.000	
V1	0.250	
V2	1.150	
Tur	0.020	
Tdr	0.010	
Tui	0.030	
Tdi	0.010	
Flag	0.000	
Imax_lim	1.000	
Imin_lim	0.770	
max_err	0.500	
min_err	-0.500	
Tvd	0.250	
Vac_ref	0.960	
gamma_cf	0.000	
Tcf	0.034	
Vac_ucf	0.900	
Alpha_max_r	70.000	In GE PSLF these values are in the power flow cards; also dc margin is in Amps not pu as given here.
Alpha_min_r	5.000	
Idc_margin_r	0.000	
Alpha_min_i	110.000	
Idc_margin_i	0.100	

With the above test case set-up, the following simulations should be performed:

1. Test 1: (integration time step = 0.0005 sec)
    a. Run for one second with no-disturbance
    b. Place a fault at bus 1 (inverter side)
    c. Fault impedance X = 0.005 pu
    d. Remove fault at 1.05 seconds (i.e. 50 ms fault duration)
    e. Run to 5 seconds
2. Test 2: (integration time step = 0.0005 sec)
    a. Run for one second with no-disturbance
    b. Place a fault at bus 4 (rectifier side)
    c. Fault impedance X = 0.005 pu
    d. Remove fault at 1.05 seconds (i.e. 50 ms fault duration)
    e. Run to 5 seconds
3. Test 3
    a. Play the waveforms for voltage (frequency is constant) shown in Figure 3 in as a source at bus 1 (inverter side) and bus 4 (rectifier side), respectively.
    b. The frequency is constant at 60 Hz on both sides
    c. The voltage on the rectifier side (bus 4) is constant at its initial value of 1.025 pu
    d. The voltage on the inverter side (bus 1) is constant at 1.047 pu from 0 to 1.0005 seconds; falls to 0.8 pu from 1.0005 seconds to 1.05 seconds; and is again constant at 1.047 pu from 1.0505 seconds to 2 seconds.
    e. The waveforms (and the simulation) are sampled at 0.0005 second intervals.
4. Test 4
    a. Play the waveforms for voltage (frequency is constant) shown in Figure 4 in as a source at bus 1 (inverter side) and bus 4 (rectifier side), respectively.
    b. The frequency is constant at 60 Hz on both sides
    c. The voltage on the inverter side (bus 1) is constant at its initial value of 1.047 pu
    d. The voltage on the rectifier side (bus 4) is constant at 1.025 pu from 0 to 1.0005 seconds; falls to 0.8 pu from 1.0005 seconds to 1.05 seconds; and is again constant at 1.025 pu from 1.0505 seconds to 2 seconds.
    e. The waveforms (and the simulation) are sampled at 0.0005 second intervals.

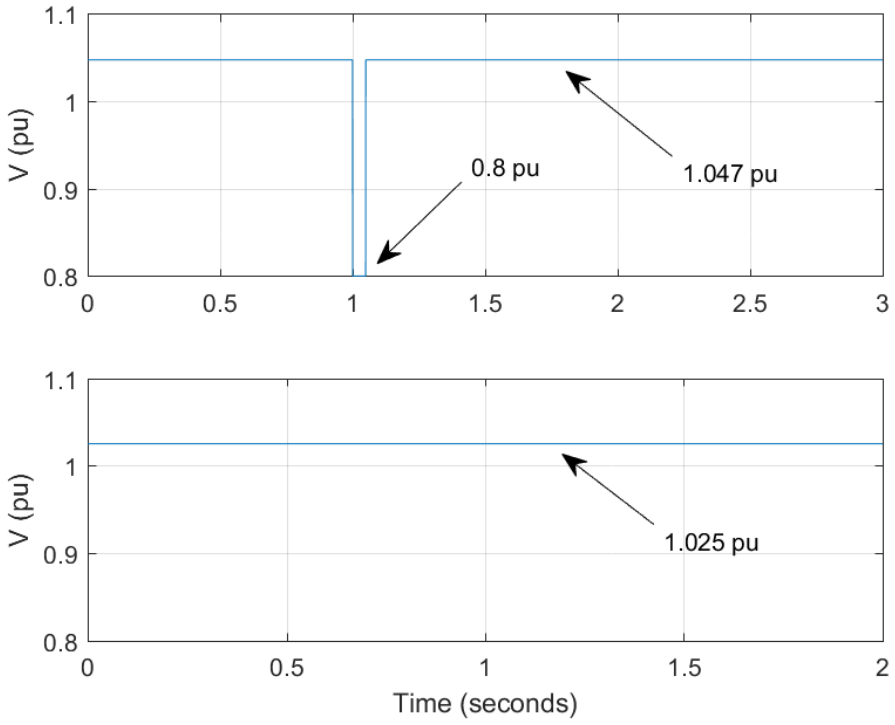

Figure 3: Voltage waveforms for Test 3.

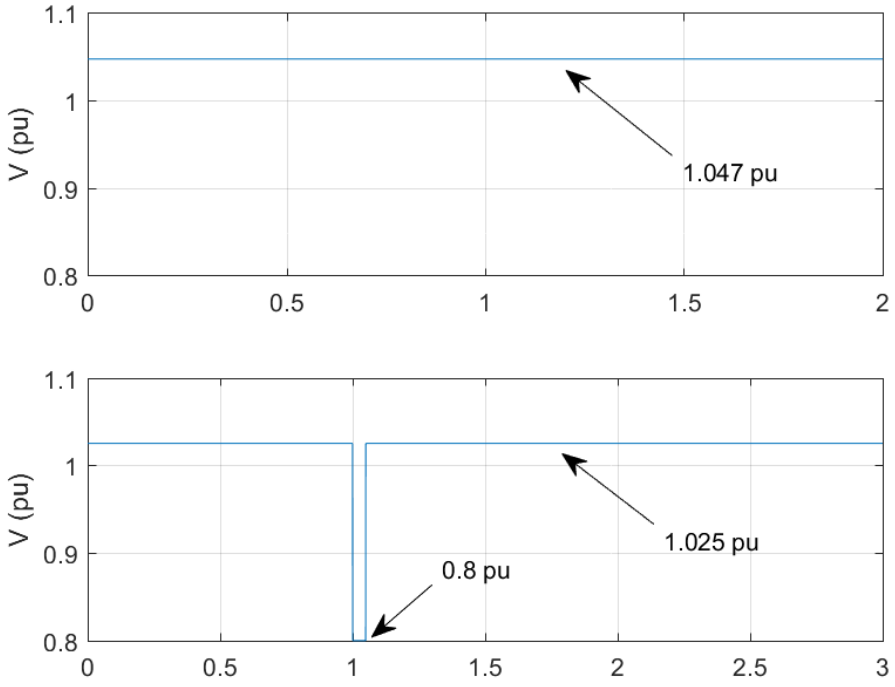

Figure 4: Voltage waveforms for Test 4.

A few ***important notes*** are pertinent at this point:

- Although, as is clear from the simulation results since gamma goes to zero, in the case of the inverter fault more than likely there would be commutation failure, for this simulation we deliberately choose ***NOT*** to emulate commutation failure (by invoking inverter bypass). This is to keep the comparison of the tests as simple as possible.

- The test case is based on the CIGRE benchmark case [5] as a starting point, however, some significant changes were made for our purposes here.

    - The test case in [5] was primarily developed for use in electromagnetic transient (EMT) type programs and so has main circuit data (e.g. specific filter bank elements) which are not relevant to power flow and stability modeling (e.g. the filter banks are represented here as a fixed, lumped shunt capacitor, neglecting filter inductive and resistive elements).

    - The test case in [5] is based on a 50 Hz system, whereas the one here is a 60 Hz equivalent.

    - Some aspects of the model in [5] are not specified or pertinent to establishing a useful power flow and stability simulation set (e.g. MVA rating and parameters for equivalent generators for the two AC systems) and so these have been defined here using reasonable, assumed, values.

    - Some parameters were changed to result in a more simple and reasonable power flow solution for the test case used here (e.g. lumped capacitors used in [5] to emulate line charging are neglected, and some of the line parameters were rounded off etc.).

    - The power flow direction in our case here is reversed compared to [5]. This is not particularly of much importance or consequence, but should be noted (i.e. in the test case here the inverter is on the 345-kV side).

2.2 Test Results for the CHVDC2 Model Across Three Software Platforms

The results of the test simulations listed above are shown in this section. All the results were obtained using GE PSLF™, PowerWorld Simulator and PowerTech Labs TSAT. These simulations were performed in September 2017. We performed the initial simulations in GE PSLF™, and shared the results and test case with the other software vendors, who very graciously then performed the same simulations on their respective platforms and sent the ASCII output files back, which were then used to develop the plots shown here.

In all the plots below the SOLID lines are GE PSLF™, the DOTTED lines are PowerWorld Simulator and DASHED lines are PowerTech Labs TSAT.

It is difficult to see the difference between the SOLID, DOTTED and DASHED lines below, because the results match quite closely across the three (3) commercial software platforms. Below is a single example (expanded) plot to show that there is some small difference, but this is attributable to unavoidable numerical differences across different software. Thus, clearly the three (3) software platforms match very well and the model behaves as expected. These results were

also observed by the members of the WECC HVDC TF, which include representatives from the major vendors and HVDC equipment, namely, ABB, Siemens, GE and Mitsubishi.

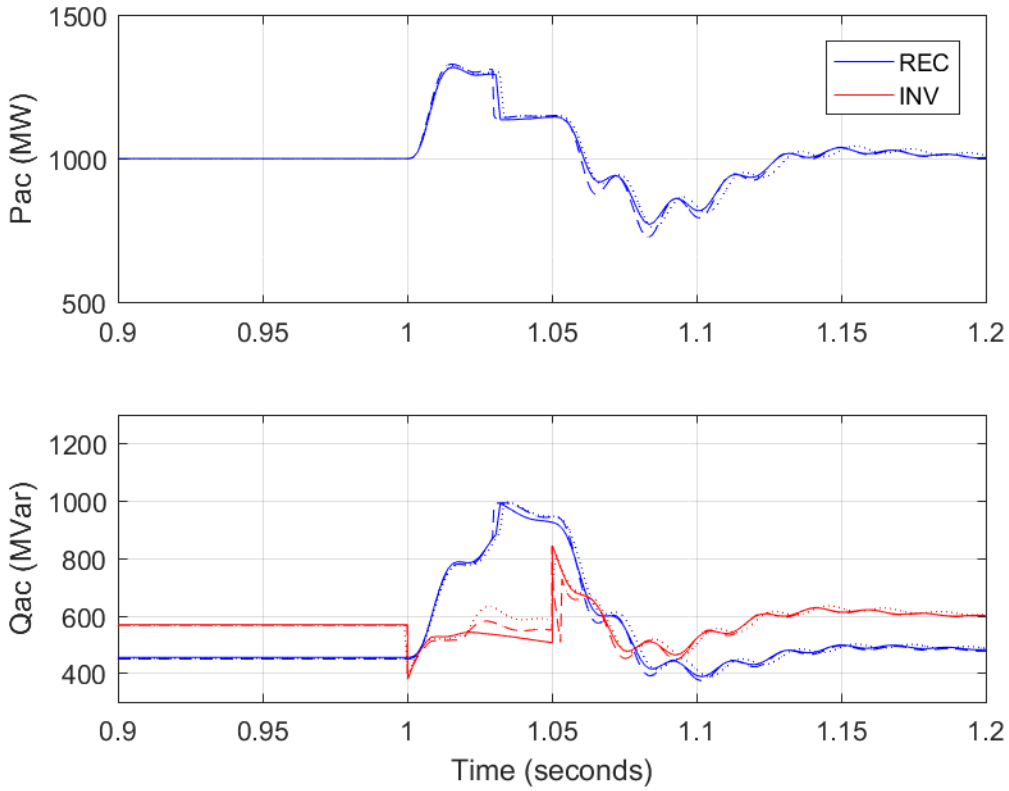

Figure 5: Zoomed in comparison of results for one case across the three (3) software platforms.

Test 1 – Inverter Side Fault

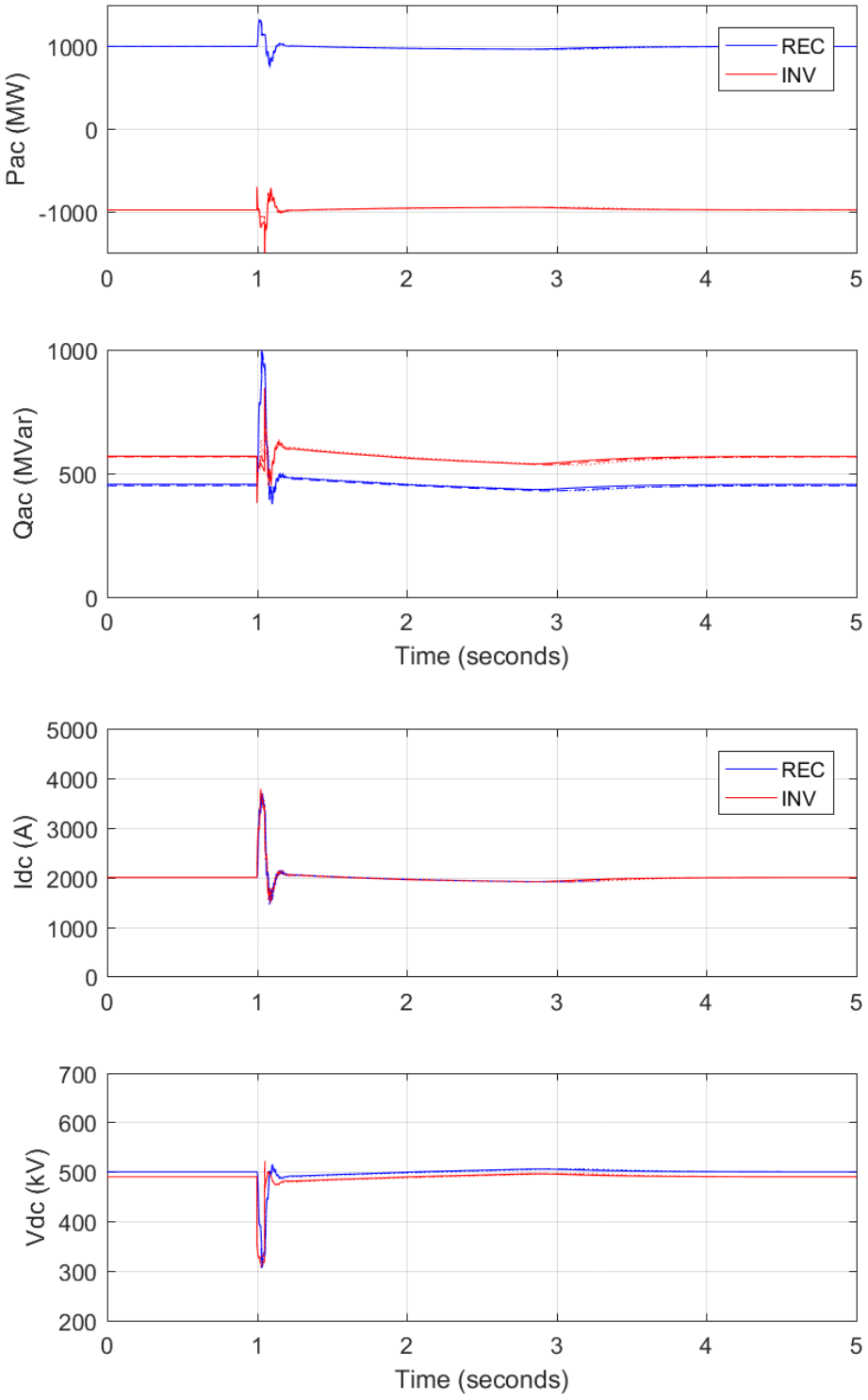

Figure 6: Test 1 – inverter side fault (P, Q, Vdc and Idc)

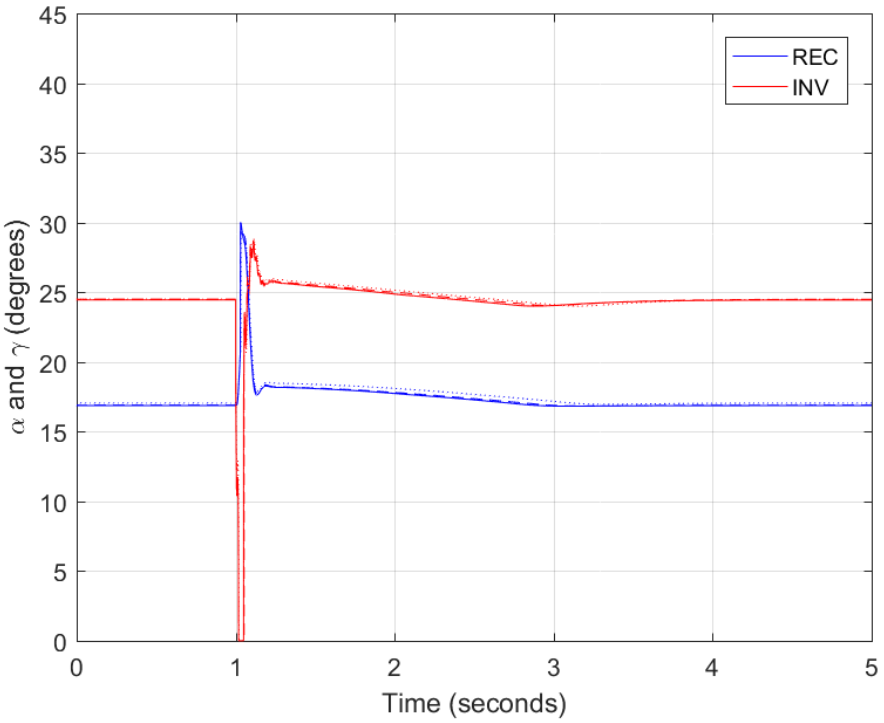

Figure 7: Test 1 – inverter side fault (alpha and gamma).

Test 2 – Rectifier Side Fault

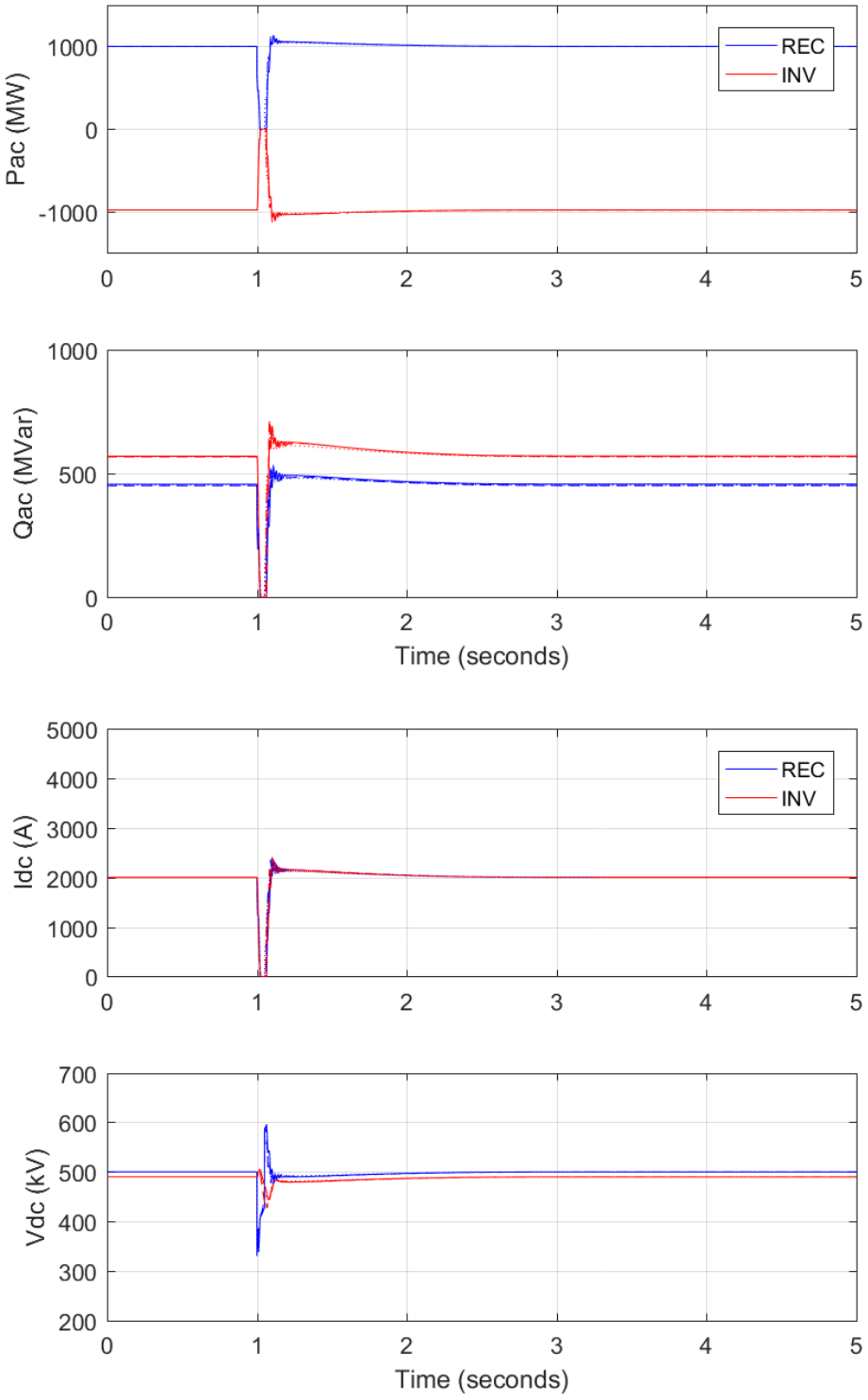

Figure 8: Test2 – rectifier side fault (P, Q, Vdc and Idc).

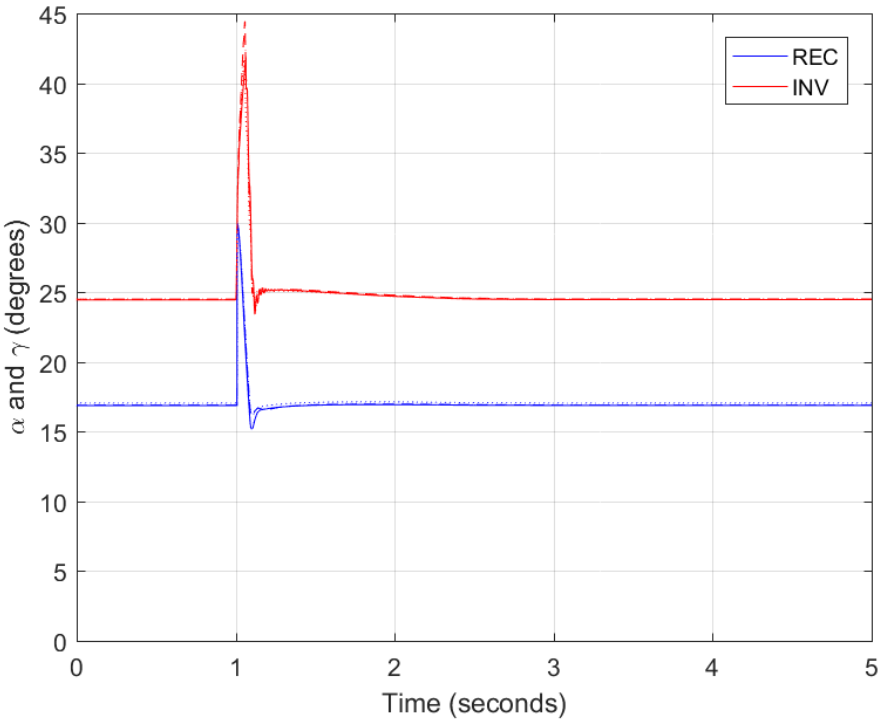

Figure 9: Test2 – rectifier side fault (alpha and gamma).

Test 3 – Inverter Side Voltage Playback

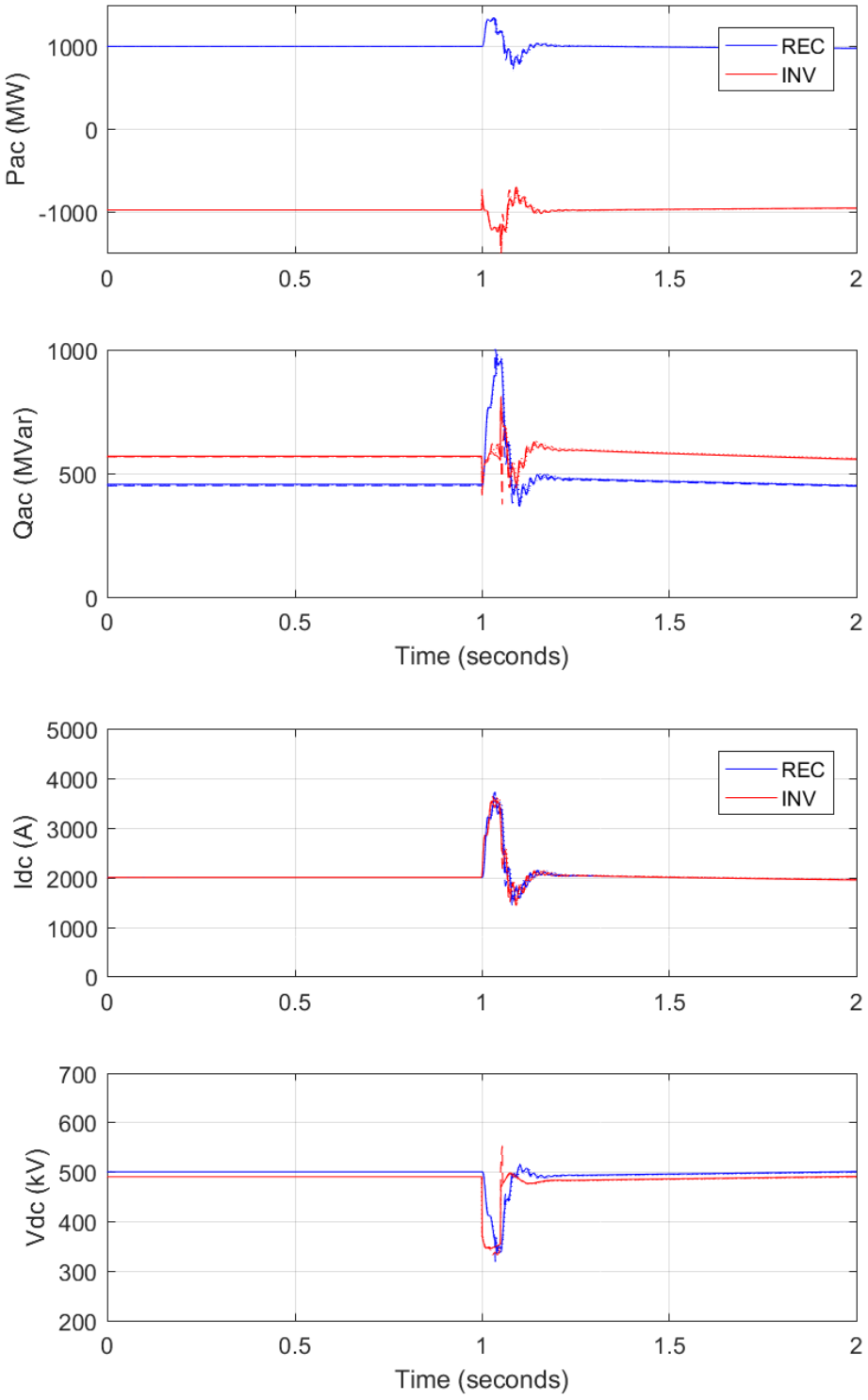

Figure 10: Tes3 – inverter side voltage play-back (P, Q, Vdc and Idc).

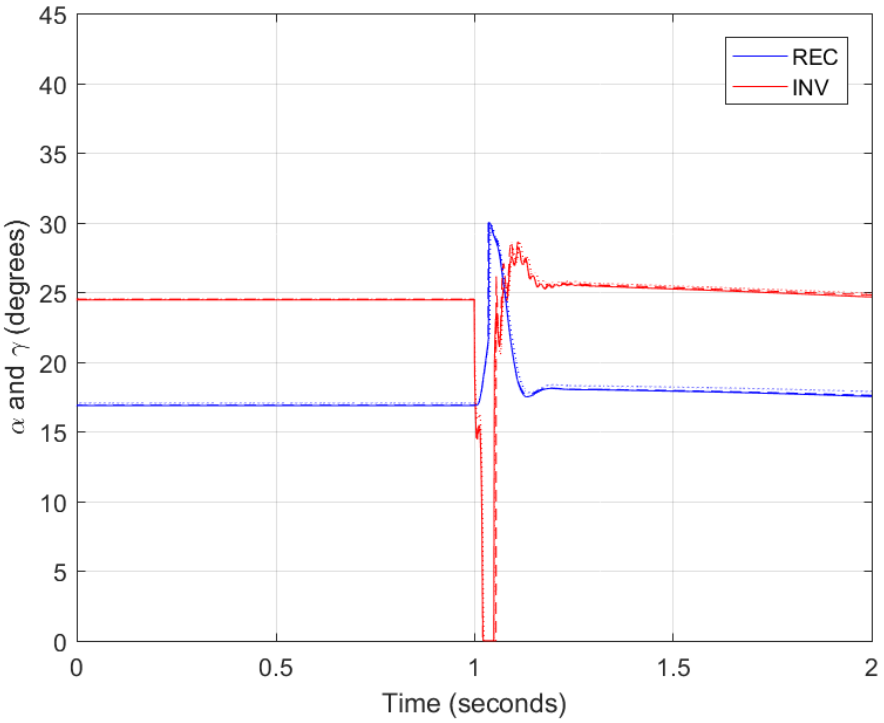

Figure 11: Tes3 – inverter side voltage play-back (alpha and gamma).

Test 4 – Rectifier Side Voltage Playback

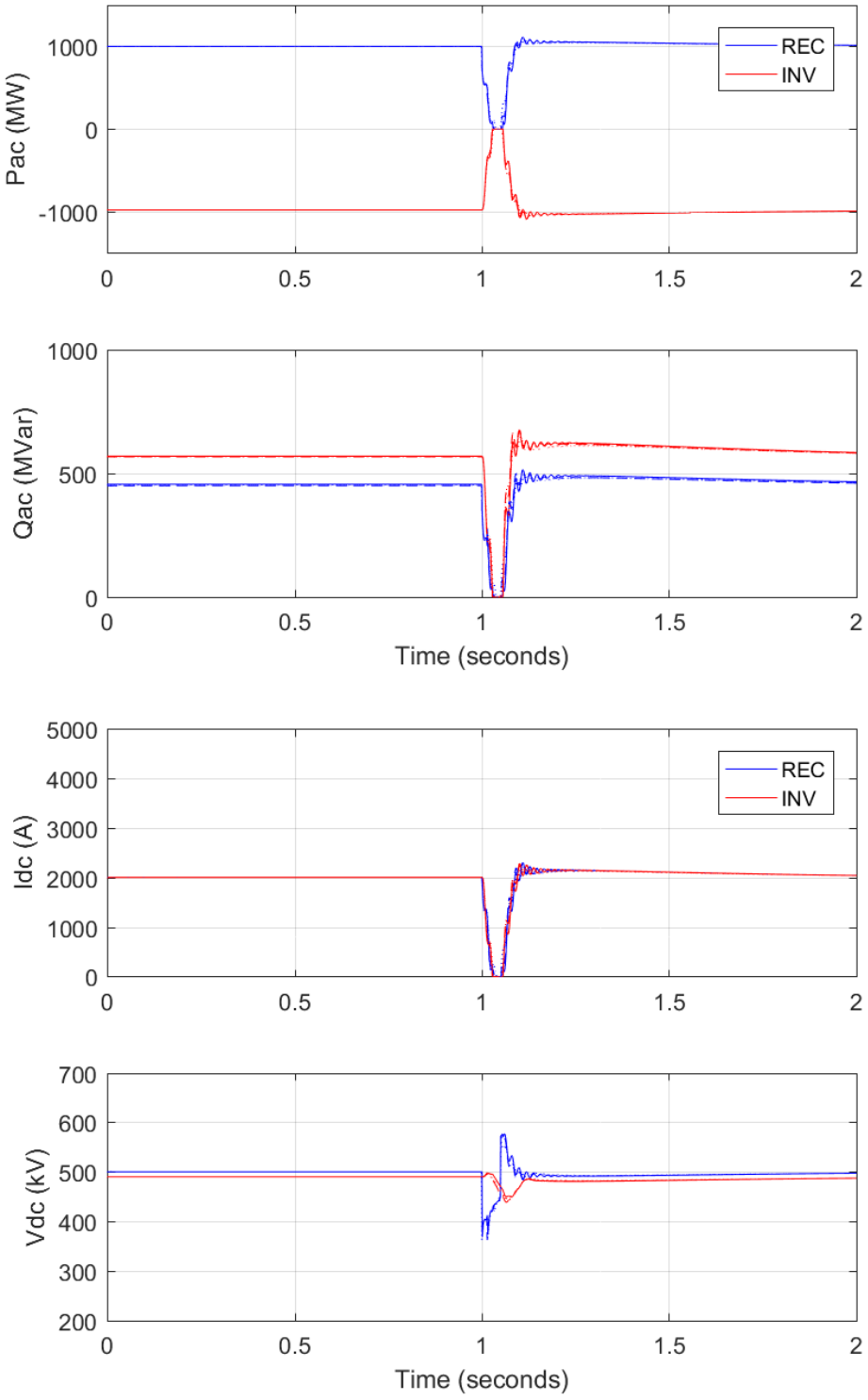

Figure 12: Tes4 – rectifier side voltage play-back (P, Q, Vdc and Idc).

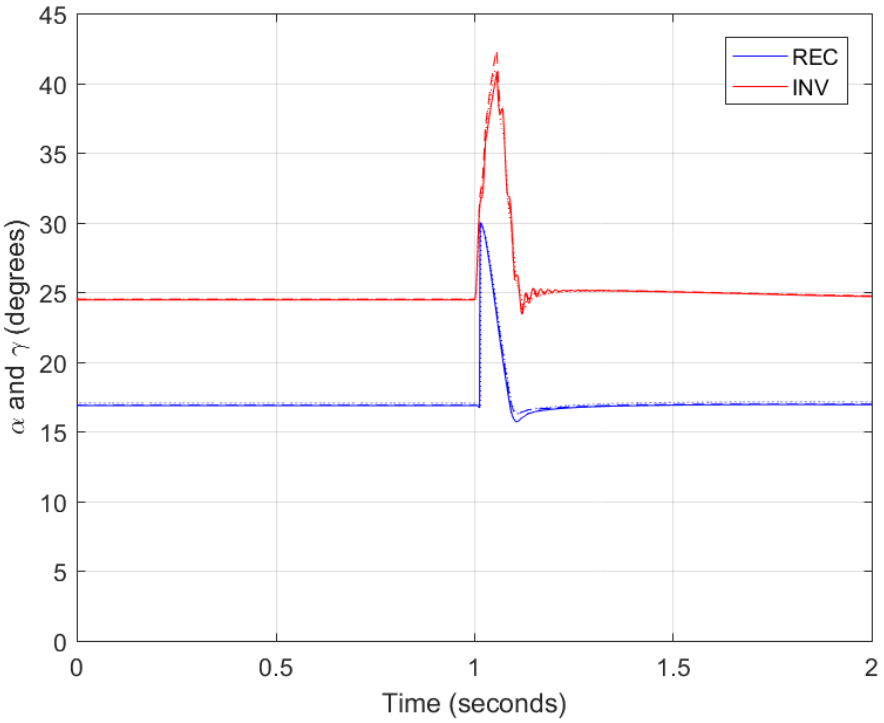

Figure 13: Tes4 – rectifier side voltage play-back (alpha and gamma).

3
CONTINUED WORK OF THE VSC HVDC DYNAMIC MODEL

The development of the dynamic model for the VSC HVDC is still in progress. In December 2015, a concept was first presented for a simple planning level VSC HVDC model. This concept was further developed in 2016 and presented as a more detailed proposal with block diagrams which were included in last year's report [6], the details of which we will thus not repeat here. By late 2016, work started on implementing this model as a user-written model in GE PSLF™ for testing the concept, but the implementation was not fully completed. As of writing this report, the coding of the user-written model has been completed and initial debugging done to be able to start performing some simulations. However, the model is not yet performing as expected and further debugging and effort is needed to fully complete this first proposal. Once that is done, simulations will be performed on a similar simple test case as for the LCC HVDC model and presented for discussion within the WECC HVDC TF seeking broad industry feedback, particularly from the equipment and software vendors. Once consensus is achieved, the model will then go through a similar process of testing and final approval and release as the LCC HVDC dynamic model. Thus, this work will continue in 2018.

4
SUMMARY, CONCLUSION AND CONTINUED WORK

This technical update provides a summary of the work done in 2017 on HVDC model development. As shown, the work on the simple and standard LCC HVDC dynamic model, called *chvdc2*, is now complete. Three (3) major commercial software platforms have already adopted and release the model in their latest software revisions, and tests have shown good agreement across these platforms. A fourth major software platform is expected to complete implementation of the model by year end. The model has also been approved by WECC and placed on WECC's approved dynamic model list.

Work continued on the development of a user-written version, in GE PSLF^{TM}, for an initial proposal for a simple VSC HVDC dynamic model. The model is yet to be completely finalized and tested. This work will continue in 2018.

5
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