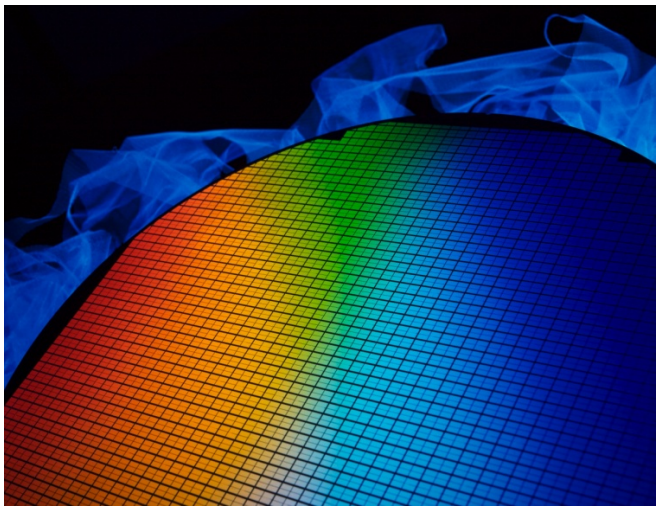
EPRI | ELECTRIC POWER RESEARCH INSTITUTE

System Compatibility Requirements for the Semiconductor Industry



- Understand electric service quality requirements
- Identify post-SEMI F47 mechanisms for continued downtime reduction of semiconductor processing equipment through industry collaboration
- Determine key strategies and methodologies to further harden semiconductor equipment to power quality events
- Inform development of revised standards, equipment designs, power system requirements, and PQ testing methodologies for current and next generation semiconductor tools
- Improve productivity through minimizing production downtime

Background, Objectives, and New Learning

Market demand for high-performance, high-value semiconductors used in today's smart phones, tablets, laptops, and other information-technology equipment is once again experiencing growth—with a revenue increase from $300 billion USD in 2010 to a projected $490 billion in 2019.

Despite significant strides to improve system compatibility in semiconductor manufacturing through the implementation of the SEMI F47 standard, there is still a significant opportunity to reduce power quality-related downtime even further. Although certified to SEMI F47, tooling equipment continues to exhibit sensitivities that lead to process upsets and high downtime costs. The success of the original EPRI effort in the semiconductor industry illustrates that, through working together, electric utilities and industry can address these issues resulting in potentially profound benefits.

The key objective of this project is to determine the characteristics of power quality events still causing semiconductor plant process downtime, take a new look at the sensitivities in the process equipment, and determine any required adjustments to equipment design or standards to further reduce voltage-sag-induced losses by the semiconductor industry.

New learnings from this project will likely include:

- Identification of root causes of remaining power quality-related downtime of semiconductor plants
- Development of effective strategies to further improve system compatibility between the equipment and electrical environment
- Determination of societal benefits to semiconductor fabrication plants (fabs) from implementation of improved compatibility methodologies

New learning from this work is also intended to be disseminated to funders of EPRI's Program 1, Power Quality.

Benefits

This important work aims to help utilities, semiconductor manufacturers, and tooling equipment providers to better understand the tolerance and susceptibility of today's generation of semiconductor processing tools and then to develop effective strategies to improve uptime and lower product losses due to single- and multi-phase voltage sag events. Furthermore, this research may provide public benefits through increased understanding and the development of new methodologies to make semiconductor processing equipment more robust to voltage sag anomalies.

Project Approach and Summary

This project intends to methodically investigate the potential factors that continue to cause semiconductor plant downtime in a post-SEMI F47 environment. These factors include: (1) three-phase voltage sag events; (2) repeated voltage sag events due to recloser operations; (3) events outside SEMI F47 scope of magnitude, duration, phase-shift or point-on-wave; (4) voltage sag testing methods utilized during certification; (5) tool software, design, or configuration differences; or (6) electrical system differences between the certification environment and the actual fab environment. Working through EPRI, it is intended that utility members work with their semiconductor site clients to investigate SEMI F47 requirements against specific site electrical environments, and identify potential gaps against tool shutdown data. It is planned that SEMI F47 certification documents be reviewed for the sensitive tool sets, and characterization of this equipment be accomplished through additional analysis and testing. The aim is also that specific design and mitigation strategies, including related cost-benefits, be determined and documented. The general, non-confidential findings from these partnerships will help inform the overall collaborative effort through workshops, white papers, and the final report. The overall effort intends to include participation in project web-meetings and workshops, inclusion in engagement with SEMI, and involvement in any proposed standards modifications.

Deliverables

Intended deliverables include, quarterly project webcast updates, at least one to two white papers and draft proposed updates to SEMI standards, annual workshops and proceedings, and the final project report.

Price and Project Structure

The project collaborative price is $100k over a two-year period which can be funded at $50k per year. The project may be funded via SDF or co-funding.

Project Status and Schedule

The funding opportunity is available now. The project is expected to last 24 months from start to finish.

Who Should Join

Electric utilities that want to support semiconductor manufacturers to improve system compatibility and minimize power quality production impacts.

Contact Information

For more information, contact the EPRI Customer Assistance Center at 800.313.3774 (askepri@epri.com).

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