Coordinated Voltage Regulating Equipment and Smart Inverter Settings with High Levels of DER

Technical Brief — *Distribution Operations and Planning*

Introduction

In distribution networks, voltage regulation has traditionally been achieved by using voltage regulation equipment (VRE) which includes feederhead voltage regulators, load tap changers (LTCs), line voltage regulators (LVRs), and shunt capacitor banks. Distribution utilities have well-established practices for siting, sizing, and configuring the control settings for VREs to regulate feeder voltages within the standard ranges [1]. However, the proliferation of distributed energy resources (DER) is forcing utility planning engineers to re-think the traditional practices, including configuring VRE setpoints. In addition, introduction of the IEEE Standard 1547-2018 [2] provides DER with smart inverter (SI) opportunity to participate in voltage regulation through advanced functionalities like constant power factor operation, volt-var (VV) mode, combined volt-var volt-watt (VV-VW) mode. However, using these advanced functionalities also increases the complexity of coordinating these new assets with conventional VREs, potentially leading to ineffective voltage and/or reactive power control [3].

There is a body of research focused on optimizing the operation of voltage regulation equipment with smart inverters [3-5]. However, the approaches commonly used involve formulating and solving complex optimization problems and assume an ADMS with bi-directional communications to all VRE and smart inverters. Such optimal control methods are possible but can be challenging to implement. Therefore, instead of complex optimization formulations, the guidance provided in this report is based on practical formulations and steps that can be utilized with information and software tools readily available to distribution planning engineers today.

This report builds upon prior research work by EPRI [6], which proposed an approach to adjust the voltage setpoints of voltage regulators to avoid overvoltage due to DER generation operating at unity power factor. Furthermore, this report provides a practical process to mitigate voltage violations caused by DER generation by also adjusting capacitor banks[1] and the settings of VREs in coordination with smart inverter functions.

There is a range of possible approaches for coordinating VRE with smart inverters shown in Figure 1 that include:

- Historically, utilities have considered adjustments to VRE control settings without considering smart inverter functions (light blue line in Figure 1).
- Alternatively, it is possible to consider smart inverter functions without adjustments to VRE control settings (pink line in Figure 1). This approach has been the focus of prior research [7-12] that has assessed the impact and value of smart inverter functions on feeder voltage regulation, reactive power demand, losses, regulator tap operations, etc. largely without considering changes to VRE control settings.
- Last, it is possible to consider both functionalities through appropriate coordination and sequencing (red line in Figure 1 considers adjusting smart inverter (SI) settings first. In contrast, the dark blue line in Figure 1 considers changing VRE control first). However, when both functionalities are considered, it is unclear how they should be coordinated and the sequence of adjustments.

The guidance provided in this report is intended to serve the full range of different approaches allowing each utility to follow the approach that best suits their circumstances. This report assumes that the functionalities considered, and their sequence has been chosen separately. The following section discusses guidance and methods to coordinate VRE and SI control settings. The section after that presents several examples applying the proposed guidance. The final section summarizes the takeaways and next steps.

Guidance to Adjust Control Setpoints

This report coordinates VRE and SI setting adjustments to mitigate voltage violations based on the functionalities and their sequence chosen by the utility following the design process illustrated in Figure 2.

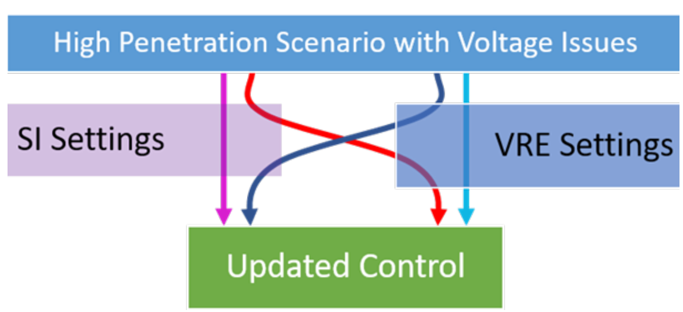


Figure 1. Four approaches to coordinate VRE with smart inverters

[1] For shunt capacitor banks, this work is limited to three-phase single-step shunt capacitor banks.

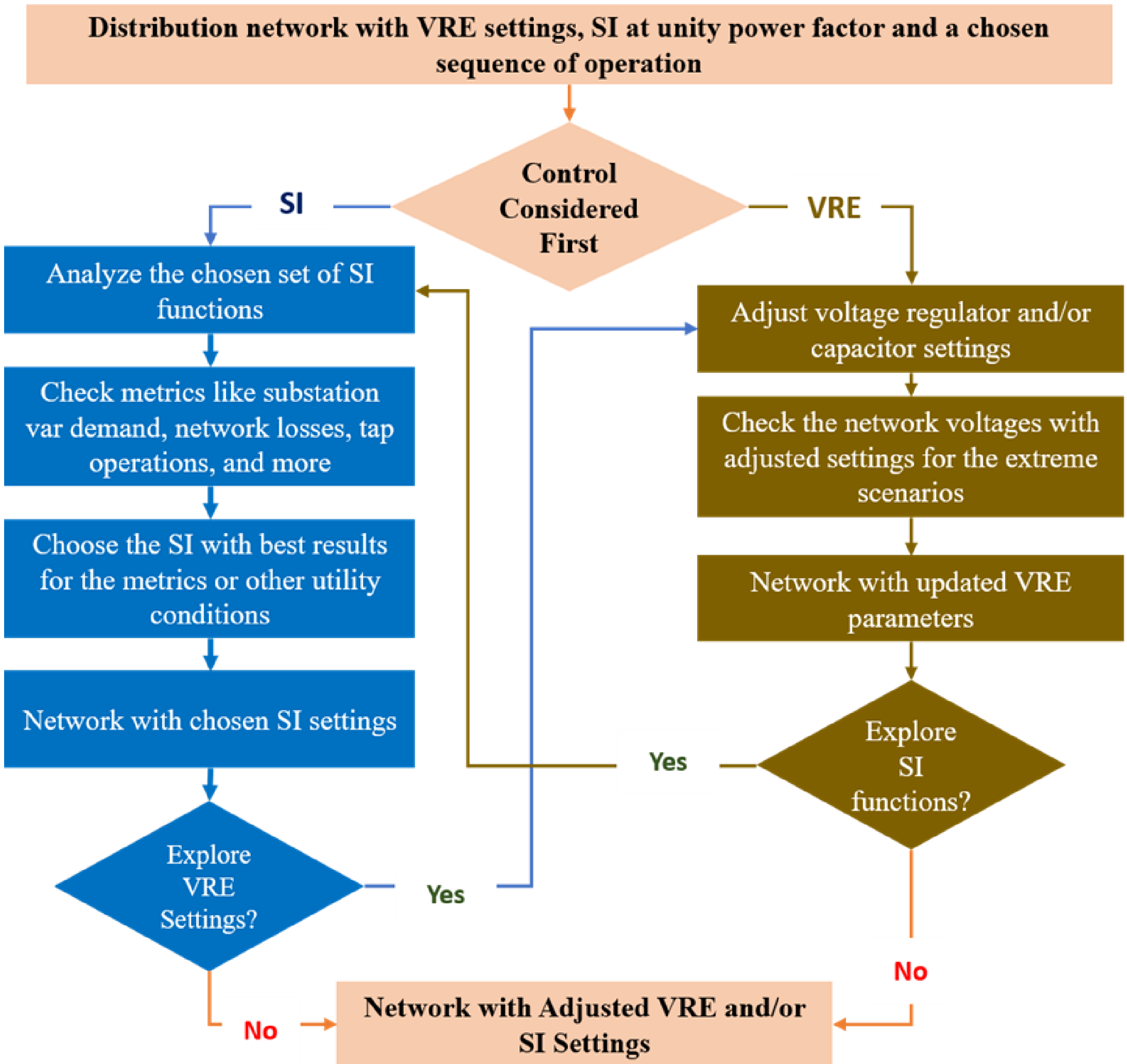


Figure 2. Coordinating VRE and SI for mitigating voltage violation

If existing VREs are considered first, then the SI functions are leveraged only if the VRE setting adjustments are insufficient. However, considering SI functions first will reverse the process, and the VRE setpoints are adjusted only if the chosen SI function is insufficient to mitigate voltage violation. The following describes the methods to select the setpoints for VREs and SIs.

The setpoints chosen for VREs and SIs must lead to proper operation in all operating conditions. The four following power flow scenarios can help to identify the worst-case voltages:

- ***Scenario 1***: Peak load without generation
- ***Scenario 2***: Minimum load without generation
- ***Scenario 3***: Peak load with nameplate rated generation output
- ***Scenario 4***: Minimum load with nameplate rated generation output

The voltages simulated for these four scenarios, intended to capture the maximum and minimum feeder voltage conditions, are used in this report as conservative estimates for adjusting VRE and SI setpoints.

The following sections provide a process for adjusting voltage regulator and capacitor bank settings and choosing SI functions. Each individual adjustment is performed separately without considering the other setting adjustments. However, it may be reasonable to consider VRE setting adjustments first given the larger impact VREs have on feeder-wide voltages.

While each of the steps below is expected to individually help mitigate voltage violations, better results are obtained by combining the steps. Therefore, evaluating the impact of different combinations for the four conservative worst-case scenarios is recommended as the most practical combination of steps varies based on circumstances.

Adjusting Voltage Regulator Setpoints

Voltage regulators that may experience reverse power flow due to DER[2] should have activated the appropriate reverse operating mode, e.g., the "co-generation" mode. In co-generation mode, the VRs continue to regulate the load side voltage upon detecting reverse power flow with separate reverse LDC settings [11]. This report guides adjusting the following VR control parameters:[3]

- Forward setpoint: V_{reg_f}
- Forward LDC settings: R_f , X_f
- Reverse setpoint: V_{reg_r}
- Reverse LDC settings: $R_r X_r$

Adjusting Forward Voltage Setpoint

It may be possible to mitigate overvoltages caused by DER generation by reducing the forward voltage setpoint of the upstream regulator. However, adjusting V_{reg_f} to a lower setpoint will affect the voltage profile in all conditions with forward power flow through the regulator, including during high load with low generation. Therefore, V_{reg_f} must be defined to avoid overvoltage conditions created by the generation during forward power flow while still preventing undervoltage conditions in heavy load conditions. Hence, V_{reg_f} can be decreased by ΔV_{reg_f} following Equation 1 on a 120 V base [6]:

$$0.5V_{bw_f} \leq \Delta V_{reg_f} \leq 120(v_{min} - v_{low}) - 0.5V_{bw_f} \qquad \textit{Equation 1}$$

when, $120(v_{min} - v_{low}) \geq 0.5V_{bw_f}$. Here, v_{min} is the lowest simulated per unit bus voltage in the regulation zone[4] of the regulator for the four conservative worst-case scenarios, V_{bw_f} is the forward bandwidth of the regulator in volts, and v_{low} is the per unit lower voltage threshold.[5]

Adjusting Forward LDC Settings

Adjusting forward LDC settings (R_f , X_f) is not recommended for mitigating overvoltage. Reducing R_f , X_f after reducing V_{reg_f} could reduce the regulation zone voltages during forward power flow conditions but may introduce under voltages during high loading and low generation conditions. Overvoltages induced by generation more likely occur during minimum load conditions accompanied by a low forward current or reverse current. Adjusting forward LDC in either condition would have little impact on voltage regulation; therefore, changing forward LDC settings is not expected to be as effective as adjusting forward regulator setpoint, V_{reg_f}.

Adjusting Reverse Voltage Setpoint

Voltage regulators with co-generation mode activated continue controlling in the "forward direction" during reverse power flow. If the minimum voltages during reverse power flow conditions are high enough to provide room for adjustment, the reverse voltage setpoint (V_{reg_r}) can be reduced by ΔV_{reg_r} by using Equation 2 on a 120 V base.

$$0.5V_{bw_r} \leq \Delta V_{reg_r} \leq 120(v_{min_r} - v_{low}) - 0.5V_{bw_r} \qquad \textit{Equation 2}$$

when, $120(v_{min_r} - v_{low}) > 0.5V_{bw_r}$. Here, v_{min_r} is the lowest per unit voltage in the regulation zone while the regulator is experiencing reverse power flow, V_{bw_r} is the reverse bandwidth of the regulator in volts. Among the four scenarios, v_{min_r} is retrieved from the steady state power flow results for the scenarios with reverse power flow through the regulator. Note that, while adjusting v_{reg_r} the difference between forward (V_{reg_f}) and reverse voltage (V_{reg_r}) setpoints of a voltage regulator must be sufficiently small to avoid excessive tap operations every time power flow direction through the regulator changes.

Adjusting Reverse LDC Settings

Voltage reduction, as discussed previously by adjusting V_{reg_r}, can also be achieved by adjusting the reverse LDC settings (R_r, X_r). Considering the zero-reactance method (compensator is thus not sensitive to variations in power factor caused by switched capacitors, load, or SI reactive power functions [13, 14]) of selecting compensator settings, i.e., $X_r = 0$, Equation 3 can be used to adjust R_r on a 120 V base.[6]

$$R_r^{preset} \leq R_r \leq \left(120(v_{min_r} - v_{low}) - 0.5V_{bw_r}\right)\frac{I_{CT}}{I} \qquad \textit{Equation 3}$$

Here, I_{CT} is the current rating of the current transformer of the VR, I is the current when max voltage reduction ($120(v_{min_r} - v_{low}) - 0.5V_{bw_r}$) is needed, and R_r^{preset} is the original resistance value in volts of the LDC settings. The value of I can be simulated by locking regulator tap and increasing DER penetration until the maximum voltage reaches vhigh + ($v_{min_r} - v_{low} - 0.5\ V_{bw_r}/120$). Here, v_{high} can be, e.g., ANSI C84.1 service voltage range A upper limit of 1.05 *pu* or the utility design standard. Note that the impact of updating R_r will be prominent during high reverse power flow conditions as opposed to adjusting V_{reg_r} that impacts all regulator reverse power flow conditions.

Algorithm 1 shows the step-by-step process of determining the voltage regulator adjustments to mitigate violations due to inter-connected DER.

[2] For simplicity, this report does not consider the reverse power flow due to reconfiguration, which can be addressed with, e.g., the "Bias Co-generation" mode [1].

[3] The effect of adjusting VR bandwidth has been addressed in [6]. While it is important to consider DER and SI impacts on the time delays, adjusting the time delays is unlikely effective for addressing voltage violations.

[4] The regulation zone of a voltage regulator consists of the buses for which the VR is the closest upstream VR. The concept applies analogously to LTCs.

[5] For example, ANSI C84.1 service voltage range A lower limit of 0.95\ pu or the utility design standard.

[6] Based on the equations described in [13]. The justification of using R_r^{preset} as the lower limit can be found in [17].

Algorithm 1: Adjusting Voltage Regulator Set Points

Calculate the minimum and maximum voltages using steady-state power flow for the four scenarios

$v_{min} \leftarrow$ *minimum of the minimum voltages recorded from the four scenarios over the regulation zone*

$v_{low} \leftarrow 0.95$, $v_{high} \leftarrow 1.05$ *(these can be set to other values preferred by utility)*

if $120(v_{min} - v_{low}) \geq 0.5V_{bw_f}$

Calculate $0.5V_{bw_f} \leq \Delta V_{reg_f} \leq 120(v_{min} - v_{low}) - 0.5V_{bw_f}$

end if

$v_{min_r} \leftarrow$ *minimum of the minimum voltages of the scenarios with reverse power flow*

if $120(v_{min_r} - v_{low}) > 0.5V_{bw_r}$

Calculate $0.5V_{bw_r} \leq \Delta V_{reg_r} \leq 120(v_{min_r} - v_{low}) - 0.5V_{bw_r}$

end if

$v_{max} \leftarrow$ *maximum voltage recorded from scenario 4 (Minimum load with 100% generation)*

$r_{tap} \leftarrow$ *regulator's tap position from power flow results from scenario 4*

while $120(v_{min_r} - v_{low}) > 0.5V_{bw_r}$ ***do***

Disable regulator control and set load values to minimum loading values and Transformer Tap $\leftarrow r_{tap}$

Increment generation size using a fixed step, run steady state power flow and record the maximum voltage $\bar{v}$

if $\bar{v} \leq v_{high} + \left(v_{min_r} - v_{low} - {0.5V_{bw_r}}/{120}\right)$

$I \leftarrow$ *Current through the transformer*

else

Calculate $R_r^{preset} \leq R_r \leq \left(120(v_{min_r} - v_{low}) - 0.5V_{bw_r}\right)\frac{I_{CT}}{I}$

break

end if

end while

Adjusting Capacitor Control Setpoints

This section provides guidance for adjusting the following settings of voltage-controlled capacitor banks:

- Capacitor ON voltage: $V_{c_{on}}$
- Capacitor OFF voltage: $V_{c_{off}}$

Adjusting Capacitor ON Voltage

Capacitor bank ON setting should be determined to ensure that the cap banks provide required support during low voltage conditions that are likely to occur at times with low DER generation. The capacitor ON voltage can be set based on utility's traditional practices as it is not be impacted by DER generation. However, it is recommended to evaluate if the capacitor ON voltage $V_{c_{on}}$ can be lowered when 1) lowering the capacitor OFF voltage $V_{c_{off}}$ would allow mitigating voltage violations and 2) lowering $V_{c_{off}}$ is limited by the capacitor bandwidth. Adjusting $V_{c_{off}}$ is addressed next.

Adjusting Capacitor OFF Voltage

While adjusting capacitor bank OFF voltage setting $V_{c_{off}}$ may mitigate overvoltages, the setting change is limited by the difference between the capacitor bank ON and OFF voltage settings, i.e., the bandwidth. From a practical operation perspective, the capacitor bandwidth should be at least 1.5 times the expected voltage changes due to capacitor bank switching [11, 13]. Conventionally, capacitor bank bandwidth is commonly set to at least 3 or 4 V (on a 120\ V scale) [13]. To consider these practical constraints in the adjustment process, $V_{c_{off}}$ adjustment is a multi-step process.

Step 1: The first step is to run a steady-state power flow for scenario 2 (min load without generation) while the capacitor bank is deactivated. The voltage at the capacitor bank terminal is recorded ($\underline{v}_c$) and $V_{c_{off}}$ should be set higher than $\underline{v}_c / c_{pt}$, otherwise, the bank will never switch off.

Step 2: In this step, two power flows are run for scenario 2 (min load without generation) with the capacitor bank deactivated and activated, and the difference in the capacitor voltages is calculated. The process is repeated for maximum loading conditions. The minimum capacitor bandwidth $v_{c_{bw}}$ is calculated using the maximum of two differences ($v_{c\,diff}^{m}$) using Equation 4.

$$v_{c_{bw}} \geq v_{c_{diff}^{m}} \times \frac{1.5}{c_{pt}} \qquad \textit{Equation 4}$$

Therefore, $V_{c_{off}}$ should be set higher than $v_{c_{bw}} + V_{c_{on}}$. However, following step 1 generally ensures that condition shown in step 2 is fulfilled.

Step 3: In the traditional approach, the OFF voltage setting mainly depends on the minimum loading situation. However, for a distribution network with a significant generation, the traditional definition of minimum loading corresponds to scenario 3 (minimum load with full generation). Therefore, two power flows are run with load values set to minimum load, disabled capacitor control, and no generation rated nameplate generation, respectively. The voltages at the capacitor bank terminal are recorded, v_c^n and v_c^w, respectively. Assuming any voltage rise above the maximum voltage is caused by DER, $V_{c_{off}}$ is at a voltage higher than v_c^n / c_{pt} but lower than v_c^w / c_{pt}}.

Equation 5 combines these three steps to adjust $V_{c_{off}}$.

$$V_{c_{off}} = min\left[max\left(\frac{v_c}{}/c_{pt}, v_{c_{bw}} + V_{c_{on}}, v_c^n/c_{pt}\right), v_c^w/c_{pt}\right] \qquad \textit{Equation 5}$$

Choosing SI Functions

Careful selection of smart inverter functions (and settings) is very important and prior EPRI research has shown how activating appropriate smart inverter functions can provide voltage regulation for distribution grids [8, 10, 15, 16]. Steady-state power flows can be performed for the four conservative scenarios to identify functions that mitigate voltage violations. Such functions can be compared against feeder reactive power demand, losses, and other metrics. If a chosen function does not mitigate all voltage violations, VRE setting adjustments can be considered to mitigate the remaining violations. In such cases, the VRE setting adjustments can be identified following the steps described above but considering the selected SI function. Figure 2 shows the sequence of steps when SI functions are considered first, but adjustments to existing VREs are still required.

Case Study Demonstration

This section demonstrates the developed guidance on a case study utility distribution feeder. First, an overview of the case study assumptions and feeder is provided. Then, the adjustment of the control setpoints based on the provided guidance is illustrated with the VRE is selected first and then assuming that SI functions are selected first.

Case Study Overview

The following assumptions are made for the demonstration:

- Voltage regulators are assumed to have identical forward and reverse settings for bandwidth, voltage setpoint, and LDC settings initially.
- The following common smart inverter functions are considered:
  - Constant power factor (up to 0.90 lagging)
  - IEEE 1547-2018 Category B Volt-Var curve
  - IEEE 1547-2018 Category B combined Volt-Var and Volt-Watt curve

The methodology will be applied to the radial feeder shown in Figure 3. The feeder has the following properties:

- Substation Voltage Level (line-to-line) = 12.47 kV
- Non-coincident Peak Demand: 8.921 MW and 2.484 Mvar
- One 450 kvar three-phase switched capacitor bank with ON and OFF voltage settings as 118 *V* and 124 *V*
- One three-phase gang-controlled feederhead voltage regulator with the entire feeder as its regulation zone with the following parameters:
  - $V_{reg_f} = V_{reg_r} = 123$ V
  - $R_f = R_r = 2$ V
  - $v_{bw_f} = v_{bw_r} = 2$ V
  - $X_f = X_r = 0$
- A hypothetical PV deployment scenario with total installed capacity = 12.5 MVA[7]
- Each smart inverter is operating at a unity power factor and the capability is limited to 0.90 power factor (leading/lagging) with a DC-AC ratio of 1.2.

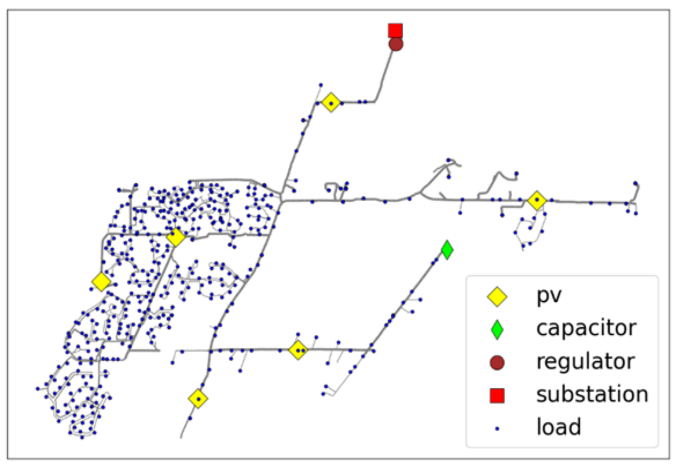
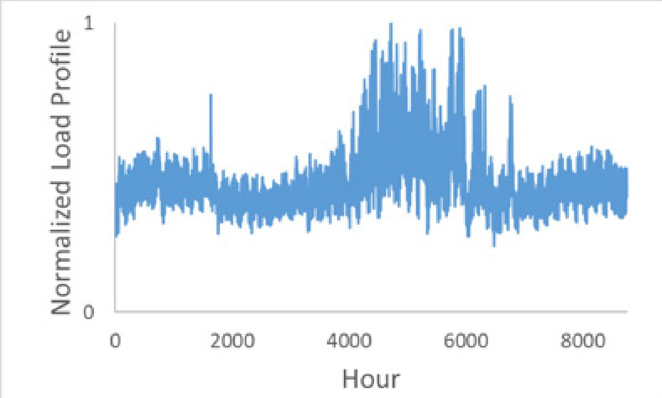


Figure 3. Case study distribution feeder with six varying sized PV installations

The yearly load profile and the solar irradiance profile used for this illustration[8] are shown in Figure 4.

[7] The hypothetical PV scenario was identified to create voltage violations, thus allowing to illustrate the setting adjustment methodology.
[8] The maximum and minimum load for the four conservative worst-case scenarios were selected based on the normalized load profile. The hourly profiles were also used for the QSTS simulations, which were not needed for the setting adjustments.



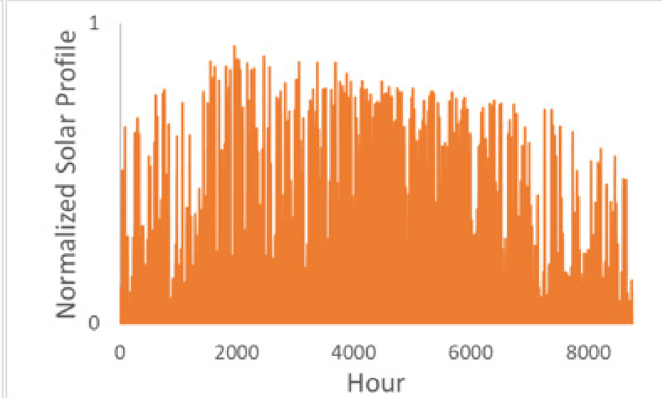


Figure 4. Normalized load (on the left) and solar irradiance (on the right) profiles

First, steady state power flows for the four scenarios are run to retrieve the minimum and maximum per unit voltages and the active power flow averaged for the phases through the voltage regulator for the conservative worst-case conditions. The results are shown in Table 1.

As shown in Table 1, overvoltages occur for Scenario 4 (midday min load with rated PV generation). These violations are confirmed with a complimentary QSTS analysis without and with PV generation shown in Figure 5. This illustrates that without PV generation the maximum and minimum voltages are within the ANSI limit, whereas with PV generation the network will experience overvoltages.

In the following section, the presented methodology will be applied to adjust the VRE and SI settings using the steady state conservative worst-case voltages listed in Table 1.

Adjustments Considering Conventional VREs First

Adjusting Regulator Setpoints

In this section, the flowchart shown in Figure 2 is described assuming that conventional VRE are adjusted first.

Regulator Forward Voltage Setpoint: Adjusting V_{regf} requires using the all-time minimum voltage, which is 0.953 *pu* from Table 1. This value does not satisfy the requirement for applying Equation 1 and therefore, no adjustment to V_{regf} can be done.

Regulator Forward LDC Settings: Based on the guidance, the LDC R_f and X_f are not adjusted.

Table 1. Minimum and maximum per unit voltages over the regulation zone (the entire feeder in this case) and regulator real power flow retrieved from steady state power flow results for the four conservative worst-case scenarios

Scenario	Load Multiplier	Min Voltage (pu)	Max Voltage (pu)	Avg VR Power Flow (kW)
Scenario 1 (Peak load without PV)	1.025	0.953	1.031	3191
Scenario 2 (Minimum load without PV)	0.229	1.013	1.030	706
Scenario 3 (Midday peak load with 100% PV generation)	1.025	0.994	1.024	-1068
Scenario 4 (Midday minimum load with 100% PV generation)	0.263	1.016	1.064	-3286

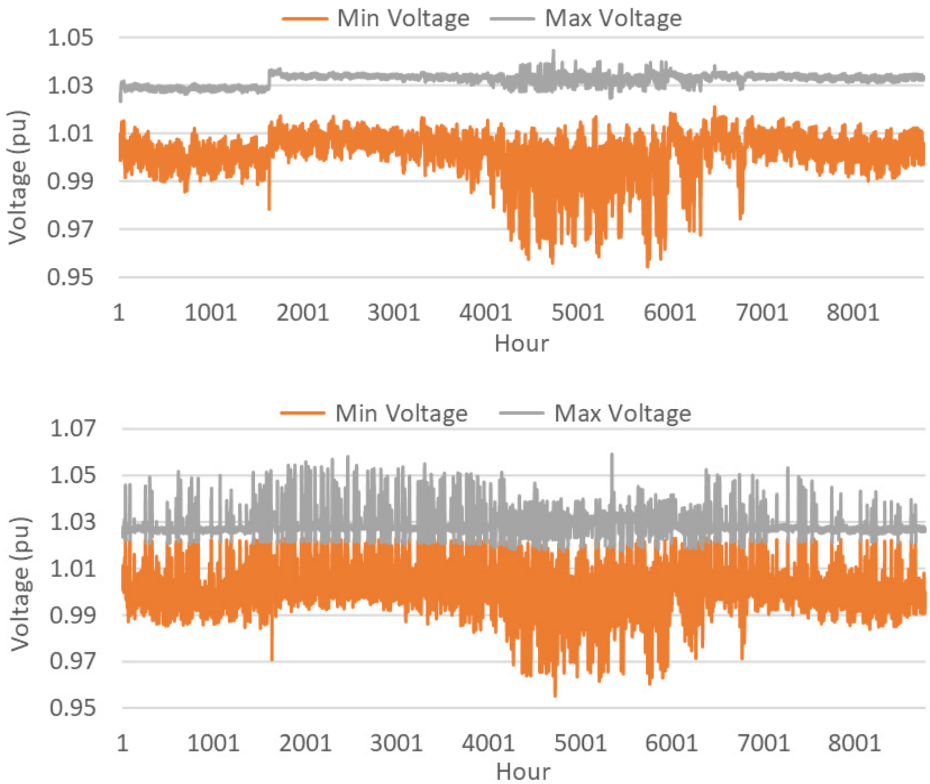


Figure 5. Hourly maximum and minimum voltages for the feeder without PV (top) and with the installed PV (bottom)

Regulator Reverse Voltage Setpoint: Applying Equation 2 requires using the minimum voltage during reverse power flow conditions. Based on the results of Scenarios 3 and 4 in Table 1, the regulator shows reverse power flow. Hence, selecting the lower minimum voltage of scenarios 3 and 4 yields $v_{min_r} = 0.995\ pu$. Using the value in Equation 2 results in the following adjustment to V_{reg_r}:

$$1 \leq \Delta V_{reg_r} \leq 4.39$$

For the demonstration below, $\Delta V_{reg_r} = 1$ V, $\Delta V_{reg_r} = 2$ V , and $\Delta V_{reg_r} = 3$ V are considered.

Regulator Reverse LDC Settings: Applying Algorithm 1 with $v_{max} = 1.064\ pu$, $I_{CT} = 500\ A$, and tap position as -1 (retrieved from the steady state results from Scenario 4), yields the following possible range for the LDC reverse resistance R_r:

$$2 \leq R_r \leq 2.59$$

For the demonstration below, $R_r = 2\ V$ and $R_r = 2.5\ V$ are considered.

Adjusting Capacitor Setpoints

Capacitor ON Voltage: The capacitor ON voltage is selected based on traditional utility practices, and therefore, for this demonstration the originally set value ($V_{c_{on}} = 118\ V$) is not changed.

Capacitor OFF Voltage: The steady state power flows required to complete the three steps to determine the OFF voltage settings resulted in the following:

Step 1: Running the steady state power flow with minimum load, no PV and the capacitor deactivated resulted in $v_c / c_{pt} = 121.75\ V$.

Step 2: The voltage difference calculated on a 120 V base for minimum loading condition and no PV scenario is 1.313 V. Calculating the same difference for maximum loading condition results in 0.533 V. Applying Equation 4 results in $v_{c_{bw}} \geq 1.969\ V$; thus $v_{c_{bw}} + V_{c_{on}} = 119.97\ V$.

Step 3: Running the two power flows described in the guidance for daytime minimum load and 0% PV and 100% PV resulted in the following:

$$v_c^n / c_{pt} = 122.8\ V;\ v_c^w / c_{pt} = 125.49\ V$$

Plugging the values calculated above in Equation 5 yields the capacitor OFF voltage setting, $V_{c_{off}} = 123\ V$.

Analyzing Impacts of the Adjustments Based on Steady-State Analysis

Various combinations of the regulator and capacitor settings adjustments determined above can be formed but some combinations may not fully mitigate voltage violations. Table 2 lists the minimum and maximum voltages obtained from steady state power flows for the four conservative worst-case scenarios for the combinations considered. As expected, several but not all adjustment combinations fully mitigated the overvoltages.[9] It is also evident from Table 2 that changing the reverse voltage setpoint V_{reg_r} has a stronger impact compared to changing R_r. The preferred setting adjustment combination can be chosen based on the utility design/engineering practices. For example, it may be preferable to choose V_{reg_r} =121 V (as opposed to V_{reg_r} =120 V) to minimize the difference between V_{reg_r} and V_{reg_f} as this is expected to reduce the regulator tap operations around the regulator power flow direction changes.

Detailed Analysis Using QSTS

Quasi-static time series (QSTS) power analysis can be useful for providing a more detailed view of the impact of the different setting adjustments on regulator and capacitor operations and other metrics. For the viable set of setting adjustment combinations shown in green in Table 2, yearly QSTS analyses are performed, and the calculated total tap operation counts and capacitor switching count are reported in Table 3. The QSTS analysis confirms that the settings adjusted based on the proposed methodology have effectively mitigated voltage violations. This also confirms that the four extreme scenarios chosen are adequate for identifying proper VRE setting adjustments.

The results shown in Table 3 also shows that the adjustment of the capacitor OFF voltage settings did not impact the capacitor operation. However, the adjustments of the regulator settings impacted the number of total tap operation counts[10] to some extent. These results can be useful for selecting the preferred settings.

Based on the results shown in Table 2, it is evident that adjusting the VRE settings only is adequate to mitigate the voltage violations due to the integrated PV. While one can still explore adjustments to SI functions, for this particular deployment of DER on this feeder of interest, it is not necessary.

Adjustments Considering SI Functionalities First

This section demonstrates the setting adjustments based on the process shown in Figure 2 assuming that SI functions are considered first. The first step is to calculate the minimum and maximum voltages for the four scenarios while considering a pre-selected set of SI functions and settings.

Table 2. Minimum and maximum per unit voltages over the regulation zone (the entire feeder in this case) and regulator real power flow retrieved from steady state power flow results for the four conservative worst-case scenarios

V_{reg_r} (V)	R_r (V)	$V_{c_{off}}$ (V)	Scenario 1		Scenario 2		Scenario 3		Scenario 4	
			Min (pu)	Max (pu)	Min (pu)	Max (pu)	Min (pu)	Max (pu)	Min (pu)	Max (pu)
122	2.5	124	0.953	1.031	1.013	1.03	0.995	1.024	1.004	1.051
		123	0.953	1.031	1.008	1.025	0.995	1.024	1.004	1.051
	2	124	0.953	1.031	1.013	1.03	0.995	1.024	1.004	1.051
		123	0.953	1.031	1.008	1.025	0.995	1.024	1.004	1.051
121	**2.5**	**124**	0.953	1.031	1.013	1.03	0.983	1.018	0.997	1.045
		123	0.953	1.031	1.008	1.025	0.983	1.018	0.997	1.045
	2	**124**	0.953	1.031	1.013	1.03	0.983	1.018	0.997	1.045
		123	0.953	1.031	1.008	1.025	0.983	1.018	0.997	1.045
120	**2.5**	**124**	0.953	1.031	1.013	1.03	0.978	1.018	0.985	1.032
		123	0.953	1.031	1.008	1.025	0.978	1.018	0.985	1.032
	2	**124**	0.953	1.031	1.013	1.03	0.978	1.018	0.991	1.039
		123	0.953	1.031	1.008	1.025	0.978	1.018	0.991	1.039

[9] The red marked adjustments in Table 4 2 does not show a complete mitigation of voltage violation, however, the changes marked in green show that the adjustments are able to mitigate the voltage violations. The adjustments marked in the red show improvement compared to Table 2 as the maximum voltage for Scenario 4 reduced from 1.06 to 1.051. However, the adjustment is not sufficient to mitigate the violation completely.

[10] The total tap count for a regulator = $\sum_{t=1}^{t=8759} |\tau_{t+1} - \tau_t|$; where τ_t is the regulators tap position at time step t; and $-16 \le \tau_t \le 16$.

Table 3. QSTS analysis results for the selected adjustments

V_{reg_r} (V)	R_r (V)	$V_{c_{off}}$ (V)	Total Tap Operation Count	Total Capacitor Switching Count
121	2.5	124	2271	83
		123	2271	83
	2	124	2115	53
		123	2115	53
120	2.5	124	3001	331
		123	3001	331
	2	124	2849	277
		123	2849	277

The results for the selected scenarios are listed in Table 4. All power factors mitigated the overvoltages, but 90% lagging power factor resulted in undervoltages due to excessive reactive power consumption by the inverters. Hence, selecting a power factor between 0.92 and 0.98 would mitigate all voltage violations without the need for adjustments to the conventional VRE settings.

Table 4. Minimum and maximum per unit voltage using steady state power flow for conservative worst-case scenarios and selected SI functions and settings

	SI Function		Minimum Voltage (pu)	Maximum Voltage (pu)
Scenario 1 (Peak load without PV)	None		0.953	1.031
Scenario 2 (Minimum load without PV)	None		1.013	1.030
Scenario 3 (Midday peak load with 100% PV generation)	Power Factor Control (lagging)	0.90	0.948	1.015
		0.92	0.958	1.019
		0.94	0.960	1.016
		0.96	0.963	1.014
		0.98	0.97	1.013
	VV Control		0.995	1.024
	VV-VW Control		0.995	1.024
Scenario 4 (Midday minimum load with 100% PV generation)	Power Factor Control (lagging)	0.90	0.998	1.015
		0.92	1.002	1.022
		0.94	1.005	1.024
		0.96	1.009	1.034
		0.98	1.011	1.042
	VV Control		1.012	1.051
	VV VW Control		1.012	1.051

To demonstrate the combined SI and VRE setting adjustment methodology, assume that VV-VW is selected. As shown in Table 4, VV-VW does not fully mitigate the overvoltages for the hypothetical deployment scenario used for this illustration.[11] Hence, the VRE settings are adjusted following the flowchart in Figure 2. Analogous to Table 1, steady state power flow analysis was performed for the four conservative worst-case scenarios with VV-VW function activated yielding the max and min voltages listed in Table 5.

Adjusting Regulator Setpoints

Regulator Forward Voltage Setpoint: Adjusting V_{reg_f} requires using the all-time minimum voltage, which is 0.953 *pu* from Table 5. This value does not satisfy the requirement for applying Equation 1 and therefore, no adjustment to V_{reg_f} can be done.

Regulator Forward LDC Settings: Based on the guidance, the LDC R_f and X_f are not adjusted.

Regulator Reverse Voltage Setpoint: Applying Equation 2 requires using the minimum voltage during reverse power flow conditions. Based on the results for Scenarios 3 and 4 in Table 5, the regulator shows reverse power flow. Hence, selecting the lower minimum voltage of Scenarios 3 and 4 yields $v_{min_r} = 0.995\ pu$. Using the value in Equation 2 results in the following adjustment to V_{reg_r}:

$$1 \leq \Delta V_{reg_r} \leq 4.39$$

For the demonstration below, $\Delta V_{reg_r} = 1\ V$, $\Delta V_{reg_r} = 2\ V$, and $\Delta V_{reg_r} = 3\ V$ are considered.

Regulator Reverse LDC Setting: Based on the methodology, X_r is set to zero. Applying Algorithm 1 with $v_{max} = 1.051\ pu$, $I_{CT} = 500\ A$, and tap position of -1 (retrieved from the steady-state results from Scenario 4), yields the following possible range for the LDC reverse resistance R_r:

$$2 \leq R_r \leq 0.932$$

As no R_r value can satisfy both constraints, R_r cannot be adjusted and hence, $R_r = R_r^{preset} = 2\ V$.

Adjusting Capacitor Setpoints

Capacitor ON Voltage: The capacitor ON voltage is selected based on traditional utility practices, and therefore, for this demonstration, the originally set value ($V_{c_{on}} = 118\ V$) is not changed.

Capacitor OFF Voltage: The steady-state power flows required to complete the three steps to determine the OFF voltage settings resulted in the following:

$$v_c/c_{pt} = 121.75\,V;\ v_{c_{bw}} + V_{c_{on}} = 119.96\,V;\ v_c^n/c_{pt} = 122.8\,V;\ v_c^w/c_{pt} = 124.8\,V$$

Applying Equation 5 on the above-calculated values results in $V_{c_{off}} = 123\ V$.

Steady-State Power Flow Results

The results for the four scenarios with the VV-VW function activated and with different combinations of adjustments to V_{reg_r} and $V_{c_{off}}$ are shown in Table 6. The preferred setting adjustment combination can be chosen based on the utility design/engineering practices (for example, minimizing the difference between V_{reg_f} and V_{reg_r}) considering the coordination between the conventional VRE and smart inverters.

Detailed Analysis Using QSTS

To provide more detail on the impact of the setting adjustments and verify snapshot results, QSTS power flow simulations were performed for the viable set of setting adjustments in Table 6. The resulting total regulator tap operation count and capacitor switching count are listed in Table 7. Figure 6 compares the regulator and capacitor operation for selected valid settings in Table 3 and Table 7. Clearly, activating the SI function has effectively reduced the regulator and capacitor operations. These results indicate that the presented methodology can be helpful in identifying effective VRE setting adjustments with or without smart inverter functions.

Table 5. Minimum and maximum per unit voltages over the regulation zone and the average power flow through the voltage regulator retrieved from steady state power flow results for the four conservative worst-case scenarios with VV-VW function activated

Scenario	Minimum Voltage (pu)	Maximum Voltage (pu)	Average flow through the regulator (kW)
Scenario 1 (Peak load without PV)	0.953	1.031	3191
Scenario 2 (Minimum load without PV)	1.013	1.030	706
Scenario 3 (Midday peak load with 100% PV generation)	0.995	1.024	-1068
Scenario 4 (Midday minimum load with 100% PV generation)	1.012	1.051	-3273

[11] For practical purposes, the max voltage of 1.051 p.u. may be acceptable but here, VRE setting adjustments are considered for demonstration purposes.

Table 6. Minimum and maximum per unit voltage for the four conservative worst-case scenarios under the combination of adjustments with VV-VW control mode activated

V_{reg_r} (V)	R_r (V)	$V_{c_{off}}$ (V)	Scenario 1		Scenario 2		Scenario 3		Scenario 4	
			Min (pu)	Min (pu)	Max (pu)	Min (pu)	Min (pu)	Max (pu)	Min (pu)	Max (pu)
122	**2**	**124**	0.953	1.031	1.013	1.03	0.995	1.024	1.007	1.048
		123	0.953	1.031	1.008	1.025	0.995	1.024	1.007	1.048
121	**2**	**124**	0.953	1.031	1.013	1.03	0.983	1.018	0.996	1.041
		123	0.953	1.031	1.008	1.025	0.983	1.018	0.996	1.041
120	**2**	**124**	0.953	1.031	1.013	1.03	0.978	1.018	0.99	1.037
		123	0.953	1.031	1.008	1.025	0.978	1.018	0.99	1.037

Table 7. QSTS analysis results for the selected SI setting adjustments

V_{reg_r} (V)	R_r (V)	$V_{c_{off}}$ (V)	Total Tap Operation Count	Total Capacitor Switching Count
122	2	124	359	9
		123	359	9
121	2	124	1235	47
		123	1235	47
120	2	124	2087	271
		123	2087	271

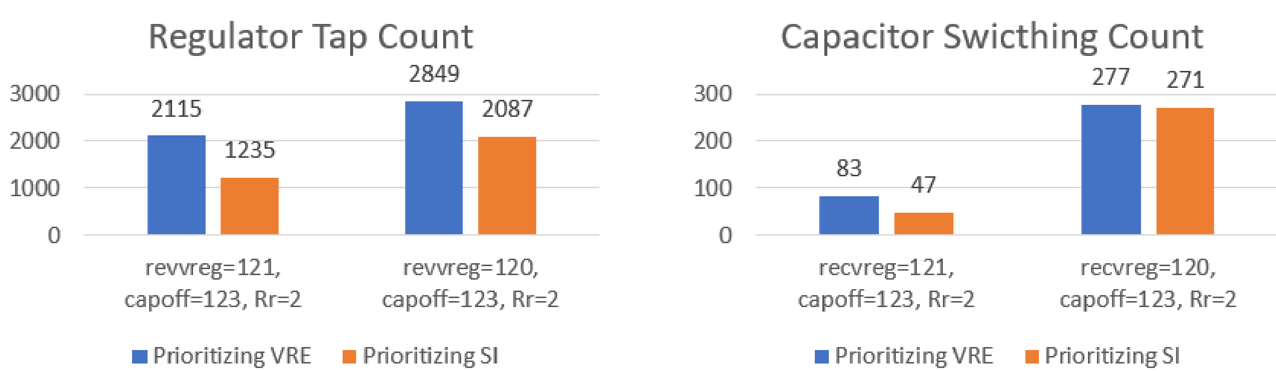


Figure 6. Comparing regulator tap count and capacitor switching count for similar adjustments with and without SI function (VV-VW control in this case)

Conclusion

Effective coordination of conventional voltage regulation equipment controls with DER and smart inverters is challenging, but it is an important topic as many utilities are facing higher penetrations of DER and reduced VRE regulating headroom. Past research has evaluated optimization based methods to identify optimal states for voltage regulation equipment and, in some cases, smart inverters. However, to implement such optimization-based methods, requires an ADMS with bi-directional communications to voltage regulation equipment and potentially smart inverters. As a result, optimization-based methods cannot be applied by most utilities today and hence, this report focused on practical methods that require a minimal modeling effort. This report provides guidance on configuring the controls of traditional VRE and smart inverters independently but goes further to guide engineers on practical approaches to coordinate the control between VRE and smart inverters. The practical guidance contained herein is applicable to the distribution planners today. The adjustment of smart inverters and/or traditional VRE control settings is focused on:

- Sequencing which equipment control should be updated first
- Requirements of when combined controls should be utilized
- Processes on how to analyze and derive combined control settings

Specific guidance on control adjustments detailed within this document requires:

- Four steady-state power flow simulations for conservative worst-case conditions
- Hand calculations to derive modified settings for traditional voltage regulation equipment

The methodology was applied to a case study feeder, and the results show that the settings adjusted based on the proposed process effectively mitigated voltage violations caused by high DER penetration. Additionally, QSTS simulations were performed to verify the adjustments based upon the snapshot analysis while providing additional details on regulator and tap operations. The methodology was applied to PV systems. Energy storage and other DER that can both import and export power would require a re-assessment of the methodology to assure it appropriately establishes settings for all operating conditions.

Future research could extend the guidance provided in this report for adjusting voltage regulator bandwidth, coordinating time delays, and adjusting multi-step capacitor banks. Future research could also involve demonstrating the developed methodology on additional feeders and scenarios, evaluating the impact of available monitoring, considering additional types of DER, and more.

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